Agilent Technologies

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GENESYS Synthesis-SPECTRASYS Link

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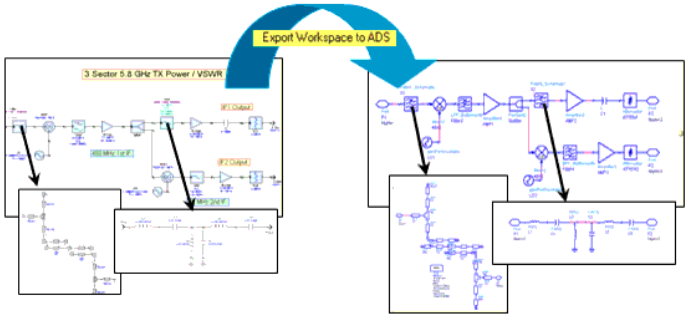
About GENESYS Synthesis-SPECTRASYS Link

This section introduces you to the GENESYS Synthesis/SPECTRASYS Link, installation and licensing, and details where to find documentation.

GENESYS Synthesis/SPECTRASYS Link Overview

Unique technology from Eagleware's GENESYS platform is now accessible from within your ADS Design Flow. Invoke the GENESYS Synthesis/SPECTRASYS link tools from your ADS session, then transfer schematics back to ADS when you are done (real time). The link includes streamlined licensing that is compatible with ADS.

- Evaluate RF system architecture
- Synthesize lower level components and re-analyze system
- Transfer design hierarchy to ADS
- Finish design & verify system specifications in ADS



GENESYS Synthesis

Application coverage of GENESYS Synthesis includes automatic design of the following circuits:

- Active (op-amp) filters
- Group delay equalization
- Multi-stage matching networks
- Distributed filters
- Active and passive mixers
- VCO and stable oscillators
- LC filters
- Splitters, couplers and attenuators
- Advanced direct LC synthesis
- Physical <-> Electrical

Note
Not all designs will transfer, see *Troubleshooting* (genlink), for more information.

SPECTRASYS

is the industry's first continuous spectrum simulator. DC-to-daylight spectrum at every node. Includes unique "Spectral Propagation and Root Cause Analysis" (SPARCA). SPECTRASYS goes beyond "budget" tools and spreadsheets to help you fix RF architecture problems that other methods never find. Exports most RF block diagrams directly to ADS schematics.

Note
Not all designs will transfer, see *Troubleshooting* (genlink), for more information.

Installation & Licensing Issues

Installation

The GENESYS Synthesis/SPECTRASYS link requires:

- An installed version of GENESYS 2006.10 or newer, which can be installed from a disk or downloaded from http://www.agilent.com/find/eesof-knowledgecenter .
- An installed version of ADS 2006A or newer. For ADS installation information, see *Installing Advanced Design System on Windows* (instalpc).

Note
The GENESYS Synthesis/SPECTRASYS link is available only on Windows based operating systems.

Licensing

If GENESYS was purchased as an ADS add-on, choose *ADS style* licensing in GENESYS. On multi-CPU machines, with both GENESYS and ADS simulation windows active, ADS will check out an extra sim_linear license and may yield an error message.

Note
On multi-CPU systems which use network licenses, it is important to always:

- Stop the ADS simulator before launching GENESYS.
- Exit GENESYS before starting a simulation in ADS.

Important
To share the same bundle between different EEsof products a user will have to set their license preference individually in each product. For example, set license preference in ADS and also set license preference in GENESYS to point to the same same bundle in order for both products to share the same bundle.

Accessing the Documentation/Training

ADS

Documentation is available on the web at:
http://www.agilent.com/find/eesof-knowledgecenter ,
or can be accessed by clicking a help button in ADS.

GENESYS

Documentation is available by selecting
Help > *Contents* or *Help* > *Index* from the main GENESYS menu. It can also be accessed by clicking an Elemental help button in GENESYS.

Training

Current course descriptions and class schedules for ADS and Eagleware-Elanix products are available from the Agilent EEsof EDA Customer Education website:
Advanced Design System (ADS) Training & Events .

Knowledge Center

Links (on the Web) to discussion forums, examples, software downloads, support documents, and tech info sessions are available from the Agilent EEsof Knowledge Center:
http://www.agilent.com/find/eesof-knowledgecenter .

Model Translation

The following section details translation information for GENESYS models to ADS.

Mapping Effects on Simulation Results

GENESYS and ADS are two distinct design environments with two distinct sets of models. During export, GENESYS models are mapped to the most similar ADS component. In most cases, the GENESYS model and the ADS component are quite similar and produce simulation results that are consistent between GENESYS and ADS. This is not always the case, though. There can be simulation differences between the GENESYS and ADS versions of a specific model. The biggest differences tend to be in transmission line discontinuity models and in SPECTRASYS models.

Mapping and Model Card/Instance Card differences

In ADS, to use a non linear device, users instantiate a model card and an instance card. The instance card references the model card. In GENESYS there is no such distinction. The parameters page for a component includes both instance and model parameters in one place.

Mapping information by section

- *Basic* (genlink)
- *Diodes* (genlink)
- *Filters* (genlink)
- *Linear* (genlink)
- *Lumped* (genlink)
- *Microstrip* (genlink)
- *Non-Simulatable Components* (genlink)
- *Stripline* (genlink)
- *System* (genlink)
- *T-Line* (genlink)
- *Transistors* (genlink)

Basic

INP (Standard Input)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *port* (anloglib) in ADS.

GENESYS Symbol	ADS Component
INPUT	Port
All other symbols	Port using the *Intermediate Subcircuit* (genlink) named genesyslib_INP_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
ZO		See note 1.
PORT	Num	
	All other ADS parameters are set to their default values.	

Notes

1. This parameter is ignored unless a TestBench is exported for the schematic. The terminations on the TestBench use the ZO from the ports.

OUT (Standard Output)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *port* (anloglib) in ADS.

GENESYS Symbol	ADS Component
OUTPUT	Port
All other symbols	Port using the *Intermediate Subcircuit* (genlink) named genesyslib_*OUT_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
ZO		See note 1.
PORT	Num	
	All other ADS parameters are set to their default values.	

Notes

1. This parameter is ignored unless a TestBench is exported for the schematic. The terminations on the TestBench use the ZO from the ports.

VDC(DC Voltage Source)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *V_DC* (ccsrc) in ADS.

GENESYS Symbol	ADS Component
VDC	V_DC
All other symbols	V_DC using the *Intermediate Subcircuit* (genlink) named genesyslib_VDC_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
VDC	Vdc	
	All other ADS parameters are set to their default values.	

Diodes

DIODE (SPICE DIODE)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *Diode* (ccnld) in ADS.

GENESYS Symbol	**ADS Component**
DIODE	genDIODE
All other symbols	genDIODE using the *Intermediate Subcircuit* (genlink) named genesyslib_DIODE_<SYMBOL>

Parameter Mapping

All GENESYS parameters are mapped to the corresponding ADS parameter. All other ADS parameters are set to their default values.

Filters

BPF_BESSEL (Bessel Bandpass Filter)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *BPF_Bessel* (ccsys) in ADS.

GENESYS Symbol	ADS Component
BPF	BPF_Bessel
All other symbols	BPF_Bessel using the *Intermediate Subcircuit* (genlink) named genesyslib_BPF_Bessel_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
IL	IL	
N	N	1 <= N <= 15
Flo		Used by Fcenter and BWpass
Fhi		Used by Fcenter and BWpass
Apass	Apass	0.01<= Apass <= 3.0
Amax	MaxRej	
Z1	Z1	
Z2	Z2	
TYPE	StopType	Set to SHORT if TYPE equals 0. Set to OPEN otherwise.
	Fcenter	(Flo + Fhi)/2
	BWpass	Flo - Fhi
	All other ADS parameters are set to their default values.	

BPF_BUTTER (Butterworth Bandpass Filter)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *BPF_Butterworth* (ccsys) in ADS.

GENESYS Symbol	ADS Component
BPF	BPF_Butterworth
All other symbols	BPF_Butterworth using the *Intermediate Subcircuit* (genlink) named genesyslib_BPF_Butter_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
IL	IL	
N	N	1<= N <= 15
Flo		
Fhi		
Apass	Apass	0.01 <= Apass <= 3.0
Amax	MaxRej	
Z1	Z1	
Z2	Z2	
TYPE	StopType	Set to SHORT if TYPE equals 0. Set to OPEN otherwise.
	Fcenter	(Flo + Fhi)/2
	BWpass	Fhi - Flo
	BWstop	Fhi - Flo
	All other ADS parameters are set to their default values.	

BPF_CHEBY (Chebyshev Bandpass Filter)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *BPF_Chebyshev* (ccsys) in ADS.

GENESYS Symbol	ADS Component
BPF	BPF_Chebyshev
All other symbols	BPF_Chebyshev using the *Intermediate Subcircuit* (genlink) named genesyslib_BPF_Cheby_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
IL	IL	
N	N	1 <= N <= 15
R	Ripple	
Flo		
Fhi		
Apass	Apass	0.01 <= Apass <= 3.0
Amax	MaxRej	
Z1	Z1	
Z2	Z2	
TYPE	StopType	Set to SHORT if TYPE equals 0. Set to OPEN otherwise.
	Fcenter	(Flo + Fhi)/2
	BWpass	Fhi - Flo
	BWstop	Fhi - Flo
	All other ADS parameters are set to their default values.	

BPF_ELLIPTIC (Elliptic Bandpass Filter)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *BPF_Elliptic* (ccsys) in ADS.

GENESYS Symbol	ADS Component
BPF	BPF_Elliptic
All other symbols	BPF_Elliptic using the *Intermediate Subcircuit* (genlink) named genesyslib_BPF_Elliptic_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
IL	IL	
N	N	1 <= N <= 15
R	Ripple	0.01 <= R <= 3.0
SBATTN	Astop	> 0
Flo		Used by Fcenter and BWpass
Fhi		Used by Fcenter and BWpass
Amax	MaxRej	
Z1	Z1	
Z2	Z2	
TYPE	StopType	Set to SHORT if TYPE equals 0. Set to OPEN otherwise.
	Fcenter	(Flo + Fhi)/2
	BWpass	Fhi - Flo
	BWstop	Fhi - Flo
	All other ADS parameters are set to their default values.	

BSF_BESSEL (Bessel Bandstop Filter)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *BSF_Bessel* (ccsys) in ADS.

GENESYS Symbol	ADS Component
BSF	BSF_Bessel
All other symbols	BSF_Bessel using the *Intermediate Subcircuit* (genlink) named genesyslib_BSF_Bessel_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
IL	IL	
N	N	1 <= N <= 15
Flo		Used by Fcenter and BWpass
Fhi		Used by Fcenter and BWpass
Apass	Apass	0.01 <= Apass <= 3.0
Amax	MaxRej	
Z1	Z1	
Z2	Z2	
TYPE	StopType	Set to SHORT if TYPE equals 0. Set to OPEN otherwise.
	Fcenter	(Flo + Fhi)/2
	BWpass	Fhi - Flo
	All other ADS parameters are set to their default values.	

BSF_BUTTER (Butterworth Bandstop Filter)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *BSF_Butterworth* (ccsys) in ADS.

GENESYS Symbol	ADS Component
BSF	BSF_Butterworth
All other symbols	BSF_Butterworth using the *Intermediate Subcircuit* (genlink) named genesyslib_BSF_Butter_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
IL	IL	
N	N	1 <= N <= 15
Flo		Used by Fcenter and BWpass
Fhi		Used by Fcenter and BWpass
Apass	Apass	0.01 <= Apass <= 3.0
Amax	MaxRej	
Z1	Z1	
Z2	Z2	
TYPE	StopType	Set to SHORT if TYPE equals 0. Set to OPEN otherwise.
	Fcenter	(Flo + Fhi)/2
	BWpass	Fhi - Flo
	BWstop	Fhi - Flo
	All other ADS parameters are set to their default values.	

BSF_CHEBY (Chebyshev Bandstop Filter)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *BSF_Chebyshev* (ccsys) in ADS.

GENESYS Symbol	ADS Component
BSF	BSF_Chebyshev
All other symbols	BSF_Chebyshev using the *Intermediate Subcircuit* (genlink) named genesyslib_BSF_Cheby_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
IL	IL	
N	N	1 <= N <= 15
R	Ripple	
Flo		Used by Fcenter and BWpass
Fhi		Used by Fcenter and BWpass
Apass	Apass	0.01 <= Apass <= 3.0
Amax	MaxRej	
Z1	Z1	
Z2	Z2	
TYPE	StopType	Set to SHORT if TYPE equals 0. Set to OPEN otherwise.
	Fcenter	(Flo + Fhi)/2
	BWpass	Fhi - Flo
	BWstop	Fhi - Flo
	All other ADS parameters are set to their default values.	

BSF_ELLIPTIC (Elliptic Bandstop Filter)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *BSF_Elliptic* (ccsys) in ADS.

GENESYS Symbol	ADS Component
BSF	BSF_Elliptic
All other symbols	BSF_Elliptic using the *Intermediate Subcircuit* (genlink) named genesyslib_BSF_Elliptic_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
IL	IL	
N	N	1 <= N <= 15
R	Ripple	0.01 <= R <= 3.0
SBATTN	Astop	
Flo		
Fhi		
Amax	MaxRej	
Z1	Z1	
Z2	Z2	
TYPE	StopType	Set to SHORT if TYPE equals 0. Set to OPEN otherwise.
	Fcenter	(Flo + Fhi)/2
	BWpass	Fhi - Flo
	BWstop	Fhi - Flo
	All other ADS parameters are set to their default values.	

HPF_BESSEL (Bessel Highpass Filter)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *HPF_Bessel* (ccsys) in ADS.

GENESYS Symbol	ADS Component
HPF	HPF_Bessel
All other symbols	HPF_Bessel using the *Intermediate Subcircuit* (genlink) named genesyslib_HPF_Bessel_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
IL	IL	
N	N	1 <= N <= 15
Fpass	Fpass	> 0
Apass	Apass	0.01 <= Apass <= 3.0
Amax	MaxRej	
Z1	Z1	
Z2	Z2	
TYPE	StopType	Set to SHORT if TYPE equals 0. Set to OPEN otherwise.
	All other ADS parameters are set to their default values.	

HPF_BUTTER (Butterworth Highpass Filter)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *HPF_Butterworth* (ccsys) in ADS.

GENESYS Symbol	ADS Component
HPF	HPF_Butterworth
All other symbols	HPF_Butterworth using the *Intermediate Subcircuit* (genlink) named genesyslib_HPF_Butter_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
IL	IL	
N	N	1 <= N <= 15
Fpass	Fpass	> 0
Apass	Apass	0.01 <= Apass <= 3.0
Amax	MaxRej	
Z1	Z1	
Z2	Z2	
TYPE	StopType	Set to SHORT if TYPE equals 0. Set to OPEN otherwise.
	All other ADS parameters are set to their default values.	

HPF_CHEBY (Chebyshev Highpass Filter)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *HPF_Chebyshev* (ccsys) in ADS.

GENESYS Symbol	ADS Component
HPF	HPF_Chebyshev
All other symbols	HPF_Chebyshev using the *Intermediate Subcircuit* (genlink) named genesyslib_HPF_Cheby_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
IL	IL	
N	N	1 <= N <= 15
Fpass	Fpass	> 0
Apass	Apass	
Amax	MaxRej	
R	Ripple	0.01 <= R <= 3.0
	Fstop	
	Astop	
Z1	Z1	
Z2	Z2	
TYPE	StopType	Set to SHORT if TYPE equals 0. Set to OPEN otherwise.
	All other ADS parameters are set to their default values.	

HPF_ELLIPTIC (Elliptic Highpass Filter)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *HPF_Elliptic* (ccsys) in ADS.

GENESYS Symbol	ADS Component
HPF	HPF_Elliptic
All other symbols	HPF_Elliptic using the *Intermediate Subcircuit* (genlink) named genesyslib_HPF_Elliptic_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
IL	IL	
N	N	1 <= N <= 15
R	Ripple	0.01 <= R <= 3.0
SBATTN	Astop	
Fpass	Fpass	> 0
Amax	MaxRej	
Z1	Z1	
Z2	Z2	
TYPE	StopType	Set to SHORT if TYPE equals 0. Set to OPEN otherwise.
	All other ADS parameters are set to their default values.	

LPF_BESSEL (Bessel Lowpass Filter)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *LPF_Bessel* (ccsys) in ADS.

GENESYS Symbol	ADS Component
LPF	LPF_Bessel
All other symbols	LPF_Bessel using the *Intermediate Subcircuit* (genlink) named genesyslib_LPF_Bessel_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
IL	IL	
N	N	1 <= N <= 15
Fpass	Fpass	> 0
Apass	Apass	0.01 <= Apass <= 3.0
Amax	MaxRej	
Z1	Z1	
Z2	Z2	
TYPE	StopType	Set to SHORT if TYPE equals 0. Set to OPEN otherwise.
	GDpass	0.9
	All other ADS parameters are set to their default values.	

LPF_BUTTER (Butterworth Lowpass Filter)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *LPF_Butterworth* (ccsys) in ADS.

GENESYS Symbol	ADS Component
LPF	LPF_Butterworth
All other symbols	LPF_Butterworth using the *Intermediate Subcircuit* (genlink) named genesyslib_LPF_Butter_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
IL	IL	
N	N	1 <= N <= 15
Fpass	Fpass	> 0
Apass	Apass	0.01 <= Apass <= 3.0
	Fstop	
	Astop	
Amax	MaxRej	
Z1	Z1	
Z2	Z2	
TYPE	StopType	Set to SHORT if TYPE equals 0. Set to OPEN otherwise.
	All other ADS parameters are set to their default values.	

LPF_CHEBY (Chebyshev Lowpass Filter)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *LPF_Chebyshev* (ccsys) in ADS.

GENESYS Symbol	ADS Component
LPF	LPF_Chebyshev
All other symbols	LPF_Chebyshev using the *Intermediate Subcircuit* (genlink) named genesyslib_LPF_Cheby_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
IL	IL	
N	N	1 <= N <= 15
Fpass	Fpass	> 0
Apass	Apass	0.01 <= Apass <= 3.0
Amax	MaxRej	
R	Ripple	
	Fstop	
	Astop	
Z1	Z1	
Z2	Z2	
TYPE	StopType	Set to SHORT if TYPE equals 0. Set to OPEN otherwise.
	All other ADS parameters are set to their default values.	

LPF_ELLIPTIC (Elliptic Lowpass Filter)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *LPF_Elliptic* (ccsys) in ADS.

GENESYS Symbol	ADS Component
LPF	LPF_Elliptic
All other symbols	LPF_Elliptic using the *Intermediate Subcircuit* (genlink) named genesyslib_LPF_Elliptic_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
IL	IL	
N	N	1 <= N <= 15
Fpass	Fpass	> 0
Apass	Apass	0.01 <= Apass <= 3.0
Amax	MaxRej	
R	Ripple	
	Fstop	
SBATTN	Astop	
Z1	Z1	
Z2	Z2	
TYPE	StopType	Set to SHORT if TYPE equals 0. Set to OPEN otherwise.
	All other ADS parameters are set to their default values.	

Linear

ONE (1-Port Data File)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *S1P* (ccsim) in ADS.

GENESYS Symbol	ADS Component
1-PORT	S1P
All other symbols	S1P using the *Intermediate Subcircuit* (genlink) named genesyslib_ONE_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
FILENAME	File	If the filename uses a relative path, you will need to edit the path so that ADS can find the file.
	Type = Touchstone	
	Interpolation Method = Linear	
	Extrapolation Method = Interpolation Mode	
	All other ADS parameters are set to their default values.	

TWO (2-Port Data File)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *S2P* (ccsim) in ADS.

GENESYS Symbol	ADS Component
2-PORT	S2P
All other symbols	S2P using the *Intermediate Subcircuit* (genlink) named genesyslib_TWO_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
FILENAME	File	If the filename uses a relative path, you will need to edit the path so that ADS can find the file.
	Type = Touchstone	
	Interpolation Method = Linear	
	Extrapolation Method = Interpolation Mode	
	All other ADS parameters are set to their default values.	

THR (3-Port Data File)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *S3P* (ccsim) in ADS.

GENESYS Symbol	ADS Component
3-PORT	S3P
All other symbols	S3P using the *Intermediate Subcircuit* (genlink) named genesyslib_THR_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
FILENAME	File	If the filename uses a relative path, you will need to edit the path so that ADS can find the file.
	Type = Touchstone	
	Interpolation Method = Linear	
	Extrapolation Method = Interpolation Mode	
	All other ADS parameters are set to their default values.	

FOU (4-Port Data File)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *S4P* (ccsim) in ADS.

GENESYS Symbol	ADS Component
4-PORT	S4P
All other symbols	S4P using the *Intermediate Subcircuit* (genlink) named genesyslib_FOU_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
FILENAME	File	If the filename uses a relative path, you will need to edit the path so that ADS can find the file.
	Type = Touchstone	
	Interpolation Method = Linear	
	Extrapolation Method = Interpolation Mode	
	All other ADS parameters are set to their default values.	

NPO<n> (n-Port Data File)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *S1P, ..., S10P* (ccsim) in ADS.

GENESYS Symbol	ADS Component
1-PORT, ..., 10-PORT	S1P, ..., S10P
All other symbols	S1P, ..., S10P using the *Intermediate Subcircuit* (genlink) named genesyslib_NPO<n>_<SYMBOL>.

Parameter Mapping

GENESYS	ADS	Comments
FILENAME	File	If the filename uses a relative path, you will need to edit the path so that ADS can find the file.
	Type = Touchstone	
	Interpolation Method = Linear	
	Extrapolation Method = Interpolation Mode	
	All other ADS parameters are set to their default values.	

Notes

1. NPO11 and higher are not mapped to ADS.

Lumped

AIRIND1 (Air Core Inductor)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *AIRIND1* (ccdist) in ADS.

GENESYS Symbol	ADS Component
INDUCTOR	AIRIND1
All other symbols	AIRIND1 using the *Intermediate Subcircuit* (genlink) named genesyslib_AIRIND1_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
N	N	
D	D	
L	L	
WD	WD	
RHO	Rho	
	Temp	Set to the ADS default value (blank)
	All other ADS parameters are set to their default values.	

CAP (Ideal Capacitor)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *C* (anloglib) in ADS.

GENESYS Symbol	ADS Component
CAPACITOR	C
All other symbols	C using the *Intermediate Subcircuit* (genlink) named genesyslib_CAP_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
C	C	
	All other ADS parameters are set to their default values.	

CAPQ (Capacitor with Q)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *CAPQ* (ccsim) in ADS.

GENESYS Symbol	ADS Component
CAPACITOR	CAPQ
All other symbols	CAPQ using the *Intermediate Subcircuit* (genlink) named genesyslib_CAPQ_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
C	C	
QC	Q	
F	F	
MODE	Mode	
RDC	RDC = 0	See note 1.
	Temp	Set to the default value (blank).
	All other ADS parameters are set to their default values.	

Notes

1. The GENESYS parameter RDC has an effect only at DC. The ADS parameter Rdc has

an effect at all frequencies.

CIR3 (Ideal 3-port Circulator)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *Circulator* (ccsys) in ADS.

GENESYS Symbol	ADS Component
CIR3	Circulator
All other symbols	Circulator using the *Intermediate Subcircuit* (genlink) named genesyslib_CIR3_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
Z	Z1 = Z	
	Z2 = Z	
	Z3 = Z	
	All other ADS parameters are set to their default values.	

DIPOLE (Dipole Antenna)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS ANTENNA documentation or refer to the documentation for *AntLoad* (ccsys) in ADS.

GENESYS Symbol	ADS Component
ANTENNA	AntLoad
All other symbols	AntLoad using the *Intermediate Subcircuit* (genlink) named genesyslib_DIPOLE_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
LEN	Length	
LD	RatioLR = 2*LD	
	AntType = DIPOLE	
	All other ADS parameters are set to their default values.	

GAIN (Ideal Gain Block)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model.

GENESYS Symbol	ADS Component
BLOCK	GAIN
All other symbols	GAIN using the *Intermediate Subcircuit* (genlink) named genesyslib_GAIN_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
A	A	
S	S = S*3.32193	Converts from db/octave to db/decade
F	F	
	All other ADS parameters are set to their default values.	

IND (Ideal Inductor)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *L* (ccsim) in ADS.

GENESYS Symbol	ADS Component
INDUCTOR	L
All other symbols	L using the *Intermediate Subcircuit* (genlink) named genesyslib_IND_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
L	L	
	All other ADS parameters are set to their default values.	

INDQ (Inductor with Q)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *INDQ* (ccsim) in ADS.

GENESYS Symbol	ADS Component
INDUCTOR	INDQ
All other symbols	INDQ using the *Intermediate Subcircuit* (genlink) named genesyslib_INDQ_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
L	L	
QL	Q	See note 1.
F	F	
MODE	Mode	See note 1.
RDC	Rdc = 0	See note 2.
	Temp	Set to the default value (blank).
	All other ADS parameters are set to their default values.	

Notes

1. For low Q (10 or less) and Mode not set to 1 (Proportional to frequency), the ADS and GENESYS simulation results start to differ for frequencies below F.
2. The GENESYS parameter RDC has an effect only at DC. The ADS parameter Rdc has an effect at all frequencies.

ISOLATOR (Ideal Isolator)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *IsolatorSML* (ccsys) in ADS.

GENESYS Symbol	ADS Component
BLOCK	IsolatorSML
All other symbols	IsolatorSML using the *Intermediate Subcircuit* (genlink) named genesyslib_ISOLATOR_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
Z	Z1 = Z	
	Z2 = Z	
	All other ADS parameters are set to their default values.	

MONOPOLE (Monopole Antenna)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *AntLoad* (ccsys) in ADS.

GENESYS Symbol	ADS Component
ANTENNA	AntLoad
All other symbols	AntLoad using the *Intermediate Subcircuit* (genlink) named genesyslib_MONOPOLE_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
LEN	Length	
LD	RatioLR	
	AntType = DIPOLE	
	All other ADS parameters are set to their default values.	

MUCQ<n> (<n> Mutually Coupled Coils)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *MUC2 thru MUC10* (ccsim) in ADS.

GENESYS Symbol	ADS Component
	MUC2 thru MUC10
All other symbols	MUC<n> using the *Intermediate Subcircuit* (genlink) named genesyslib_MUCQ<n>_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
Ln	Ln	
Kij	Kij	
Qn		Not supported by the ADS component.
RDn	Rn = 0	See note 1.
F		Not supported by the ADS component.
MODE		Not supported by the ADS component.
	Temp	Set to the default value (blank).
	All other ADS parameters are set to their default values.	

Notes

1. The GENESYS parameters RDCn have an effect only at DC. The ADS parameters Rn have an effect at all frequencies.

MUI (Two Mutually Coupled Inductors)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *MUC2* (netlist) in ADS.

GENESYS Symbol	ADS Component
MUTUAL	MUC2
All other symbols	MUC2 using the *Intermediate Subcircuit* (genlink) named genesyslib_MUI_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
L1	L1	
L2	L2	
K	K12	
	R1 = 0	
	R2 = 0	
	All other ADS parameters are set to their default values.	

OPA (Operational Amplifier)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *OpAmpIdeal* (ccsys) in ADS.

GENESYS Symbol	ADS Component
	OpAmpIdeal
All other symbols	OpAmpIdeal using the *Intermediate Subcircuit* (genlink) named genesyslib_OPA_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
RI	Rdiff	
RO	Rout	
G	Gain	
F	BW	
	All other ADS parameters are set to their default values.	

PFC (Parallel LC Resonator)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *PLCQ* (ccsim) in ADS.

GENESYS Symbol	ADS Component
PFC	PLCQ
All other symbols	PLCQ using the *Intermediate Subcircuit* (genlink) named genesyslib_PFC_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
F	$L = \frac{1}{4\pi^2 CF^2}$	
C	C	
QL	Ql	
QC	Qc	
	Fl = 1 MHz	
	ModL = Constant	
	Fc = 1 MHz	
	ModC = Constant	
	All other ADS parameters are set to their default values.	

PFL (Parallel LC Resonator)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *PLCQ* (ccsim) in ADS.

GENESYS Symbol	ADS Component
PFC	PLCQ
All other symbols	PLCQ using the *Intermediate Subcircuit* (genlink) named genesyslib_PFL_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
F	$C = \frac{1}{4\pi^2 LF^2}$	
L	L	
QL	Ql	
QC	Qc	
	Fl = 1 MHz	
	ModL = Constant	
	Fc = 1 MHz	
	ModC = Constant	
	All other ADS parameters are set to their default values.	

PLC (Parallel LC Network)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *PLCQ* (ccsim) in ADS.

GENESYS Symbol	ADS Component
PFC	PLCQ
All other symbols	PLCQ using the *Intermediate Subcircuit* (genlink) named genesyslib_PLC_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
L	L	
C	C	
QL	Ql	
QC	Qc	
	Fl = 1 MHz	
	ModL = Constant	
	Fc = 1 MHz	
	ModC = Constant	
	All other ADS parameters are set to their default values.	

PRC (Parallel RC Network)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *PRC* (ccsim) in ADS.

GENESYS Symbol	ADS Component
PRC	PRC
All other symbols	PRC using the *Intermediate Subcircuit* (genlink) named genesyslib_PRC_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
R	R	
C	C	
Qc		Not supported by the ADS component.
	Temp	Set to the default value (blank).
	All other ADS parameters are set to their default values.	

PRL (Parallel RL Network)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *PRL* (ccsim) in ADS.

GENESYS Symbol	ADS Component
PRL	PRL
All other symbols	PRL using the *Intermediate Subcircuit* (genlink) named genesyslib_PRL_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
R	R	
L	L	
QL		Not supported by the ADS component.
	Temp	Set to the default value (blank).
	All other ADS parameters are set to their default values.	

PRX (Parallel RLC Network)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the

documentation for *PRLC* (ccsim) in ADS.

GENESYS Symbol	ADS Component
PRX	PRLC
All other symbols	PRLC using the *Intermediate Subcircuit* (genlink) named genesyslib_PRX_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
R	R	
L	L	
C	C	
QL		Not supported by the ADS component.
QC		Not supported by the ADS component.
	Temp	Set to the default value (blank).
	All other ADS parameters are set to their default values.	

RES (Ideal Resistor)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *R* (circosim) in ADS.

GENESYS Symbol	ADS Component
RESISTOR	R
All other symbols	R using the *Intermediate Subcircuit* (genlink) named genesyslib_RES_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
R	R	
	All other ADS parameters are set to their default values.	

SFC (Series LC Resonator)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *SLCQ* (ccsim) in ADS.

GENESYS Symbol	ADS Component
SFC	SLCQ
All other symbols	SLCQ using the *Intermediate Subcircuit* (genlink) named genesyslib_SFC_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
F	$L = \frac{1}{4\pi^2 C F^2}$	
C	C	
QL	Ql	
QC	Qc	
	Fl = 1 MHz	
	ModL = Constant	
	Fc = 1 MHz	
	ModC = Constant	
	All other ADS parameters are set to their default values.	

SFL (Series LC Resonator)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *SLCQ* (ccsim) in ADS.

GENESYS Symbol	ADS Component
SFC	SLCQ
All other symbols	SLCQ using the *Intermediate Subcircuit* (genlink) named genesyslib_SFL_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
F	$C = \frac{1}{4\pi^2 LF^2}$	
L	L	
QL	Ql	
QC	Qc	
	Fl = 1 MHz	
	ModL = Constant	
	Fc = 1 MHz	
	ModC = Constant	
	All other ADS parameters are set to their default values.	

SLC (Series LC Network)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *SLCQ* (ccsim) in ADS.

GENESYS Symbol	ADS Component
SFC	SLCQ
All other symbols	SLCQ using the *Intermediate Subcircuit* (genlink) named genesyslib_SLC_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
L	L	
C	C	
QL	Ql	
QC	Qc	
	Fl = 1 MHz	
	ModL = Constant	
	Fc = 1 MHz	
	ModC = Constant	
	All other ADS parameters are set to their default values.	

SRC (Series RC Network)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *SRC* (ccsim) in ADS.

GENESYS Symbol	ADS Component
See note 1	SRC
All other symbols	SRC using the *Intermediate Subcircuit* (genlink) named genesyslib_SRC_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
R	R	
C	C	
Qc		Not supported by the ADS component.
	Temp	Set to the default value (blank).
	All other ADS parameters are set to their default values.	

Notes

1. The symbol for the ADS SRC component is 7/8 inch long rather than the usual 1 inch. This means that an intermediate subcircuit (called genesyslib_SRC_SRC) is used to map the 1 inch GENESYS symbol to the 7/8 inch ADS symbol.

SRL (Series RL Network)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *SRL* (ccsim) in ADS.

GENESYS Symbol	ADS Component
SRL	SRL
All other symbols	SRL using the *Intermediate Subcircuit* (genlink) named genesyslib_SRL_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
R	R	
L	L	
QI		Not supported by the ADS component.
	Temp	Set to the default value (blank).
	All other ADS parameters are set to their default values.	

SRX (Series RLC Network)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *SRLC* (ccsim) in ADS.

GENESYS Symbol	ADS Component
SRX	SRLC
All other symbols	SRLC using the *Intermediate Subcircuit* (genlink) named genesyslib_SRX_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
R	R	
L	L	
C	C	
QL		Not supported by the ADS component.
QC		Not supported by the ADS component.
	Temp	Set to the default value (blank).
	All other ADS parameters are set to their default values.	

TFC (Thin Film Capacitor)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *TFC* (ccdist) in ADS.

GENESYS Symbol	ADS Component
CAPACITOR	TFC
All other symbols	TFC using the *Intermediate Subcircuit* (genlink) named genesyslib_TFC_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
W	W	
L	L	
T	T	
Er	Er	
Rho	Rho = Rho/1.42	GENESYS is relative to copper. ADS is relative to gold.
TanD	TanD	
	All other ADS parameters are set to their default values.	

TORIND (Toroidal Core Inductor)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *CIND2* (ccdist) in ADS.

GENESYS Symbol	ADS Component
INDUCTOR	CIND2
All other symbols	CIND2 using the *Intermediate Subcircuit* (genlink) named genesyslib_TORIND_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
N	N	
AL	AL	
Rs	R	
Qc	Q	
Fq	Freq	
	All other ADS parameters are set to their default values.	

TRF (Transformer)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *TF* (ccsim) in ADS.

GENESYS Symbol	ADS Component
TRANSFORMER	TF
All other symbols	TF using the *Intermediate Subcircuit* (genlink) named genesyslib_TRF_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
P	T= P/S	
S		
OPTION		OPTION must be 0 (indicating turns rather then impedance ratio).
	All other ADS parameters are set to their default values.	

TWO (2-port data file)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *S2P* (ccsim) in ADS, or intermediate subcircuits.

GENESYS Symbol	ADS Component
see note 1	S2P
All other symbols	S2P using the *Intermediate Subcircuit* (genlink) named genesyslib_TWO_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
FILENAME	File	If the filename uses a relative path, you will need to edit the path so that ADS can find the file.
	Type = Touchstone	
	All other ADS parameters are set to their default values.	

Notes

1. The symbol for the ADS S2P component is a simple rectangle. The GENESYS TWO model is typically used with a variety of symbols, (amplifiers, BJTs, FETS, etc.) an intermediate sub-circuit is almost always used so that the GENESYS symbol appears in ADS.

XTL (Crystal)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *XTAL1* (ccdist) in ADS.

GENESYS Symbol	ADS Component
CRYSTAL	XTAL1
All other symbols	XTAL1 using the *Intermediate Subcircuit* (genlink) named genesyslib_XTL_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
R	R	
L	L	
Cm	C	
Co	Cp	
	OT = 1	
	Temp	Set to the default value (blank).
	All other ADS parameters are set to their default values.	

Microstrip

MBN (Microstrip Bend)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *MBEND2* (ccdist) in ADS.

GENESYS Symbol	ADS Component
MBN	MBEND2
All other symbols	MBEND2 using the *Intermediate Subcircuit* (genlink) named genesyslib_MBN_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
W	W	
SUBST	Subst	
	All other ADS parameters are set to their default values.	

MCN<n> (Multiple Coupled Microstrip Lines)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *PCLIN2* (ccdist), *PCLIN3* (ccdist),...,*PCLIN10* (ccdist) in ADS.

GENESYS Symbol	ADS Component
<n>-Lines	PCLIN<n>
All other symbols	PCLIN<n> using the *Intermediate Subcircuit* (genlink) named genesyslib_MCN<n>_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
W	W	
S		See note 1.
L	L	
SUBST	Subst	
	S	See note 1.
	Layer = 1	See note 1.
	All other ADS parameters are set to their default values.	

Notes

1. For ADS model PCLIN, S<n> refers to a coordinate of gaps across microstrip lines from an origin (wall), whereas for MCN, S<n> refers to a gap width. The translation between the parameters follows:
    1. (a) PCLIN.S1 = W
    2. (b) PCLIN.S<i> = W + (i * W) + Sum(MCN.S<j>, j=1...(n-1)) for i=2...n.
2. All microstrip lines lay on the same layer.

MCN4A (Asymmetric Coupled Microstrip Lines)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *MACLIN* (ccdist) in ADS.

GENESYS Symbol	ADS Component
TRL_COUPLED	MACLIN
All other symbols	MACLIN using the *Intermediate Subcircuit* (genlink) named genesyslib_MCN4A_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
W1	W1	
W2	W2	
S1	S	
L	L	
SUBST	Subst	
	All other ADS parameters are set to their default values.	

MCP (Two Coupled Microstrip Lines)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *MCLIN* (ccdist) in ADS.

GENESYS Symbol	ADS Component
TRL_COUPLED	MCLIN
All other symbols	MCLIN using the *Intermediate Subcircuit* (genlink) named genesyslib_MCP_<SYMBOL>

Parameter Mapping

GENESYS Parameter	ADS Parameter	Comments
W	W	
S	S	
L	L	
SUBST	Subst	
	All other ADS parameters are set to their default values.	

MCR (Microstrip Cross)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *MCROS* (ccdist) in ADS.

GENESYS Symbol	ADS Component
MCR	MCROS
All other symbols	MCROS using the *Intermediate Subcircuit* (genlink) named genesyslib_MCR_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
W1	WT	
W2	WC	
W3	WT	
W4	WC	
SUBST	Subst	
	All other ADS parameters are set to their default values.	

MCURVE (Microstrip Curved Bend)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *MCURVE* (ccdist) in ADS.

GENESYS Symbol	ADS Component
MCURVE	MCURVE
All other symbols	MCURVE using the *Intermediate Subcircuit* (genlink) named genesyslib_MCURVE_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
W	W	
ANG	Angle	
RAD	Radius	
SUBST	Subst	
	All other ADS parameters are set to their default values.	

MEN (Microstrip Open End)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *MLEF* (ccdist) in ADS.

GENESYS Symbol	ADS Component
MEN	MLEF
All other symbols	MLEF using the *Intermediate Subcircuit* (genlink) named genesyslib_MEN_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
W	W	
L	0 mil	
SUBST	Subst	
	All other ADS parameters are set to their default values.	

MGA (Microstrip Gap)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *MGAP* (ccdist) in ADS.

GENESYS Symbol	ADS Component
MGA	MGAP
All other symbols	MGAP using the *Intermediate Subcircuit* (genlink) named genesyslib_MGA_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
W	W	
G	S	
SUBST	Subst	
	All other ADS parameters are set to their default values.	

MLI (Microstrip Line)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *MLIN* (ccdist) in ADS.

GENESYS Symbol	ADS Component
MLI	MLIN
All other symbols	MLIN using the *Intermediate Subcircuit* (genlink) named genesyslib_MLI_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
W	W	
L	L	
SUBST	Subst	
	All other ADS parameters are set to their default values.	

MRS (Microstrip Radial Stub)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *MRSTUB* (ccdist) in ADS.

GENESYS Symbol	ADS Component
RADIAL_STUB2	MRSTUB
All other symbols	MRSTUB using the *Intermediate Subcircuit* (genlink) named genesyslib_MRS_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
R		
Phi	Angle	
W	Wi	
H		See note 1.
SUBST	Subst	
	L = R - (0.5**W/sin(Phi**PI/360))	
	All other ADS parameters are set to their default values.	

Notes

1. Parameter value is taken from the substrate.

MST (Microstrip Step)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *MSTEP* (ccdist) in ADS.

GENESYS Symbol	ADS Component
TRL_STEP	MSTEP
All other symbols	MSTEP using the *Intermediate Subcircuit* (genlink) named genesyslib_MST_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
NAR	W1	
W	W2	
OPTION		See note 1.
SUBST	Subst	
	All other ADS parameters are set to their default values.	

Notes

1. Only the symmetrical step is supported, i.e. OPTION = 0.

MTAPER (Microstrip Linearly Tapered Line)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *MTAPER* (ccdist) in ADS.

GENESYS Symbol	ADS Component
TAPER	MTAPER
All other symbols	MTAPER using the *Intermediate Subcircuit* (genlink) named genesyslib_MTAPER_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
W1	W1	
W2	W2	
LEN	L	
SUBST	Subst	
	All other ADS parameters are set to their default values.	

MTE (Microstrip Symmetrical or Asymmetrical Tee Junction)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *MTEE* (ccdist) in ADS.

GENESYS Symbol	ADS Component
TRL_TEE3	MTEE
All other symbols	MTEE using the *Intermediate Subcircuit* (genlink) named genesyslib_MTE_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
W1	W1	
W2	W2	
W3	W3	
SUBST	Subst	
OPTION		
	All other ADS parameters are set to their default values.	

MVH (Microstrip Via Hole)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *VIA* (ccdist) in ADS.

GENESYS Symbol	ADS Component
See note 1	VIA
All other symbols	VIA using the *Intermediate Subcircuit* (genlink) named genesyslib_MVH_<SYMBOL>

Parameter Mapping

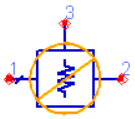
GENESYS	ADS	Comments
R	D1 = 2**R D2 = 2R**	
H	H = H	If H is not specified, the value is taken from the substrate specified by SUBST.
T	T = T	If T is not specified, the value is taken from the substrate specified by SUBST.
SUBST	Subst	See the comments for H and T.
	All other ADS parameters are set to their default values.	

Notes

1. An intermediate subcircuit is always used regardless of the symbol used in GENESYS.

Non-Simulatable Components

There are several SPECTRASYS components that have no counterpart in ADS. These components are transferred into ADS as non-simulatable components.



Non-simulatable components appear on the ADS schematic with orange circle-slashes through them.

To perform a simulation in ADS, you need to replace each instance of a non-simulatable component with an instance of a regular ADS component or with an instance of a subcircuit that you create to model the component. See *Component Mappings* (genlink) for more information.

The following GENESYS models are mapped to ADS non-simulatable components.

GENESYS Model	**GENESYS Symbol †**	**ADS Component**
ATTN_Ctrl	ATTN_DC_CTRL	NoSimATTN_Ctrl
ATTN_VAR_Linear	ATTN_VAR	NoSimATTN_VAR_Linear
ATTN_VAR_NonLinear	ATTN_VAR	NoSimATTN_VAR_NonLinear
ContFreq	CONT_SOURCE	NoSimContFreq
CWPNSource	CWPN_SOURCE	NoSimCWPNSource
CWSource	CW_SOURCE	NoSimCWSource
DIG_DIV	FREQ_DIV2	NoSimDIG_DIV
FREQ_DIV	FREQ_DIV	NoSimFREQ_DIV
IAC	IAC	NoSimIAC
IAC_PN	IAC	NoSimIAC_PN
INOISE	Inoise	NoSimINOISE
INP_PNOISE	NOISE_SOURCE	NoSimINP_PNOISE
IPULSE	IDC	NoSimIPULSE
IPWL	IDC	NoSimIPWL
LOG_DET	LOG_DET	NoSimLOG_DET
MIXER_TBL	MIXER_IF	NoSimMIXER_TBL_IF
MIXER_TBL	MIXER_RF	NoSimMIXER_TBL_RF
MulticarrierSource	MULTI_SOURCE	NoSimMulticarrierSource
PAC	PAC	NoSimPAC
RxIntermodSource	RXIM_SOURCE	NoSimRxIntermodSource
SDATA_NL	AMPL	NoSimSDATA_NL
SDATA_NL	ATTN	NoSimSDATA_NL
SDATA_NL	ATTN_VAR	NoSimSDATA_NL
SDATA_NL_HO	AMPL	NoSimSDATA_NL_HO
VAC	VAC	NoSimVAC
VarAmp	VGA	NoSimVarAmp
VNOISE	Vnoise	NoSimVNOISE
VPULSE	VDC	NoSimVPULSE
VPWL	VDC	NoSimVPWL
WidebandSource	WIDE_SOURCE	NoSimWidebandSource

† If a different symbol is used, the GENESYS model is still mapped into ADS as a non-simulatable component. In this case, an intermediate sub-circuit will be used, so you need to push inside the sub-circuit to see the non-simulatable component.

Stripline

SBCP (Offset Broadside Coupled Striplines)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *SOCLIN* (ccdist) in ADS.

GENESYS Symbol	ADS Component
TRL_COUPLED	SOCLIN
All other symbols	SOCLIN using the *Intermediate Subcircuit* (genlink) named genesyslib_SBCP_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
W	W	
WO	WO	
S	S	
L	L	
SUBST	Subst	
	All other ADS parameters are set to their default values.	

SBN (Stripline Bend)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *SBEND* (ccdist) in ADS.

GENESYS Symbol	ADS Component
SBN	SBEND
All other symbols	SBEND using the *Intermediate Subcircuit* (genlink) named genesyslib_SBN_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
W	W	
A	Angle	
SUBST	Subst	
	All other ADS parameters are set to their default values.	

SCP (Coupled Striplines)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *SCLIN* (ccdist) in ADS.

GENESYS Symbol	ADS Component
TRL_COUPLED	SCLIN
All other symbols	SCLIN using the *Intermediate Subcircuit* (genlink) named genesyslib_SCP_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
W	W	
S	S	
L	L	
SUBST	Subst	
	All other ADS parameters are set to their default values.	

SEN (Stripline Open End)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *SLEF* (ccdist) in ADS.

GENESYS Symbol	ADS Component
TRL_END	SLEF
All other symbols	SLEF using the *Intermediate Subcircuit* (genlink) named genesyslib_SEN_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
W	W	
SUBST	Subst	
	L = 0 mil	
	All other ADS parameters are set to their default values.	

SLI (Stripline)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *SLIN* (ccdist) in ADS.

GENESYS Symbol	ADS Component
TLE	SLIN
All other symbols	SLIN using the *Intermediate Subcircuit* (genlink) named genesyslib_SLI_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
W	W	
L	L	
SUBST	Subst	
	All other ADS parameters are set to their default values.	

SLIO (Offset Striplines)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *SLINO* (ccdist) in ADS.

GENESYS Symbol	ADS Component
TLE	SLINO
All other symbols	SLINO using the *Intermediate Subcircuit* (genlink) named genesyslib_SLIO_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
W	W	
L	L	
A		Used by S.
SUBST	Subst	
	S = 2 **A**	
	All other ADS parameters are set to their default values.	

SSP (Stripline Step in Width)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *SSTEP* (ccdist) in ADS.

GENESYS Symbol	ADS Component
SSP	SSTEP
All other symbols	SSTEP using the *Intermediate Subcircuit* (genlink) named genesyslib_SSP_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
NAR	W1	
W	W2	
SUBST	Subst	
	All other ADS parameters are set to their default values.	

STE (Stripline Tee Junction)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *STEE* (ccdist) in ADS.

GENESYS Symbol	ADS Component
STE	STEE
All other symbols	STEE using the *Intermediate Subcircuit* (genlink) named genesyslib_STE_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
WT	W1	
WT	W2	
SS	W3	
SUBST	Subst	
	All other ADS parameters are set to their default values.	

System

ANT_CPLD (Antenna (Coupled))

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *S2P* (ccsim) in ADS.

GENESYS Symbol	ADS Component
ANT_CPLD	genAntCpld
All other symbols	genAntCpld using the *Intermediate Subcircuit* (genlink) named genesyslib_ANT_CPLD_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
ISO	S21 = dbpolar(-abs(ISO),Phase)**-1**	
Phase	S12 = dbpolar(-abs(ISO),Phase)**-1**	
ZIN	Z1 = ZIN	
ZOUT	Z2 = ZOUT	
	S11 = 0	
	S22 = 0	
	All other ADS parameters are set to their default values.	

Notes

1. This component has been modeled as a two-port network with the parameters listed in the ADS column of the previous table.

ATTN_Linear (Attenuator (Fixed))

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *Amplifier2* (ccsys) in ADS.

GENESYS Symbol	ADS Component
ATTN	genATTN_Linear
All other symbols	genATTN_Linear using the *Intermediate Subcircuit* (genlink) named genesyslib_ATTN_Linear_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
L		See note 1.
ZIN	Amplifier2.Z1	
ZOUT	Amplifier2.Z2	
	Amplifier2.S21 = dbpolar(Gain,0)	See note 1.
	Amplifier2.S11 = dbpolar(Min_dB,0)	See note 2.
	Amplifier2.S22 = dbpolar(Min_dB,0)	See note 2.
	Amplifier2.S12 = dbpolar(Gain,0)	See note 1.
	All other ADS parameters are set to their default values.	

Notes

1. Gain = -abs(L) in dB
2. Min_dB = -316.948 in dB

ATTN_NonLinear (Attenuator (NonLinear))

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *Amplifier2* (ccsys) in ADS.

GENESYS Symbol	ADS Component
ATTN	genATTN_NonLinear
All other symbols	genATTN_NonLinear using the *Intermediate Subcircuit* (genlink) named genesyslib_ATTN_NonLinear_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
L		See note 1, 3.
ZIN	Amplifier2.Z1	
ZOUT	Amplifier2.Z2	
IP1db		See note 4.
IPSAT		See note 4.
IIP3	Amplifier2.TOI = IIP3 + Gain	See note 1.
IIP2	Amplifier2.SOI = IIP2 + Gain	See note 1.
	Amplifier2.S21 = dbpolar(Gain,0)	See note 1.
	Amplifier2.S11 = dbpolar(Min_dB,0)	See note 2.
	Amplifier2.S22 = dbpolar(Min_dB,0)	See note 2.
	Amplifier2.S12 = dbpolar(Gain,0)	See note 1.
	All other ADS parameters are set to their default values.	

Notes

1. Gain = -abs(L) in dB.
2. Min_dB = -316.948 in dB
3. Gain is used in Amplifier2.S21, Amplifier2.S12, Amplifer2.SOI and Amplifier2.TOI.
4. Both IP1dB and IPSAT are ignored, because Amplifier2 cannot specify compression along with 2nd and 3rd order intercept parameters. Generating spectral lines at the proper frequencies is more important than calculating the correct power at these frequencies. This mapping will be sufficiently accurate for input power less than IP1dB.

COUPLER1 (Single Direction Coupler)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *S3P (3-Port S-parameter File)* (ccsim) in ADS.

GENESYS Symbol	ADS Component
COUPLER1	genCOUPLER1
All other symbols	genCOUPLER1 using the *Intermediate Subcircuit* (genlink) named genesyslib_COUPLER1_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
IL		See note 2.
CPL		See note 3.
DIR		See note 4.
ZIN1	S3P.Z[1]	
ZIN2	S3P.Z[2]	
ZIN3	S3P.Z[3]	
	S11_lin = dbpolar(MinS_dB, 0)	See note 5,6.
	S12_lin = dbpolar(IL_dB, 0)	See note 2,6.
	S13_lin = dbpolar(CPL_dB, 90)	See note 3,6.
	S23_lin = dbpolar(CPL_dB+DIR_dB, 0)	See note 3,4,6.
	All other ADS parameters are set to their default values.	

Notes

1. This component has been modeled as a 3 port S-parameter block, S3P.
2. IL_dB = -abs(IL)
3. CPL_dB = -abs(CPL)
4. DIR_dB = -abs(DIR)
5. MinS_dB = -300 in dB
6. The S parameter block is set as follows: (a) all port reflection values are set to S11_lin (b) port 1 to port 2 direct transmission values are set to S12_lin (c) port 1 to port 3 coupled transmission values are set to S13_lin (d) port 2 to port 3 couplings are set to S23_lin.

COUPLER2 (Dual Direction Coupler)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *CouplerDual (Dual Coupler)* (ccsys) in ADS.

GENESYS Symbol	ADS Component
COUPLER2	genCOUPLER2
All other symbols	genCOUPLER2 using the *Intermediate Subcircuit* (genlink) named genesyslib_COUPLER2_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
IL		See note 2.
CPL1	genCOUPLER1_1.CPL = CPL1_dB	See note 3.
CPL2	genCOUPLER1_2.CPL = CPL2_dB	See note 4.
DIR1	genCOUPLER1_1.DIR = DIR1_dB	See note 5.
DIR2	genCOUPLER1_2.DIR = DIR2_dB	See note 6.
ZIN1	genCOUPLER1_1.ZIN1	
ZIN2	genCOUPLER1_2.ZIN1	
ZIN3	genCOUPLER1_1.ZIN3	
ZIN4	genCOUPLER1_2.ZIN3	
	genCOUPLER1_1.IL = IL1_dB	See note 2 thru 14.
	genCOUPLER1_2.IL = IL2_dB	See note 2 thru 13, 15.
	All other ADS parameters are set to their default values.	

Notes

1. This component has been modeled as a custom sub-circuit using two instances of the genCOUPLER1 sub-circuit, genCOUPLER1_1 and genCOUPLER1_2. Sub-circuit genCOUPLER1_1 connect port 1 to port 2, and genCOUPLER1_2 connect port 3 to port 4.
2. IL_dB = -abs(IL)
3. CPL1_dB = -abs(CPL1)
4. CPL2_dB = -abs(CPL2)
5. DIR1_dB = -abs(DIR1)
6. DIR2_dB = -abs(DIR2)
7. CPL1_lin = 0.5*real(dbpolar(CPL1_dB), 0))

8. DIR1_lin = 0.5*real(dbpolar(DIR1_dB), 0))
9. MinLoss1 = 10*log(1-(CPL1_lin+DIR1_lin))
10. CPL2_lin = 0.5*real(dbpolar(CPL2_dB), 0))
11. DIR2_lin = 0.5*real(dbpolar(DIR2_dB), 0))
12. MinLoss2 = 10*log(1-(CPL2_lin+DIR2_lin))
13. MinLoss = MinLoss1 + MinLoss2
14. IL1_dB = if 2*abs(IL_dB)<abs(MinLoss) then -abs(MinLoss1) else 0.5*IL_dB endif
15. IL2_dB = if 2*abs(IL_dB)<abs(MinLoss) then -abs(MinLoss2) else 0.5*IL_dB endif

Delay (Ideal Time Delay Block (DELAY)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *TimeDelay (Time Delay)* (ccsys) in ADS.

GENESYS Symbol	**ADS Component**
DELAY	TimeDelay
All other symbols	TimeDelay using the *Intermediate Subcircuit* (genlink) named genesyslib_Delay_<SYMBOL>

Parameter Mapping

GENESYS	**ADS**	**Comments**
T	Delay	
Z0	ZRef	
	RTConj	
	All other ADS parameters are set to their default values.	

Notes

1. This component has been modeled as an attenuator in ADS.

Duplexer_C (Duplexer with Chebyshev Filters)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *BPF Chebyshev (Bandpass Filter, Chebyshev)* (ccsys) in ADS.

GENESYS Symbol	**ADS Component**
DUPLEXER	genDuplexer_C
All other symbols	genDuplexer_C using the *Intermediate Subcircuit* (genlink) named genesyslib_Duplexer_C_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
FLOA		Used to calculate Fcenter and BWpass
FHIA		Used to calculate Fcenter and BWpass
FLOB		Used to calculate Fcenter and BWpass
FHIB		Used to calculate Fcenter and BWpass
NA	BPFA.N	
NB	BPFB.N	
RA	BPFA.Ripple	
RB	BPFB.Ripple	
ILA	BPFA.IL	
ILB	BPFB.IL	
Apass	BPFA.Apass, BPFB.Apass	
Amax	BPFA.MaxRej, BPFB.MaxRej	
Zin	S3P1.Z[1], BPFA.Z1, BPFB.Z1	
Zout	BPFA.Z2, BPFB.Z2	
	BPFA.Fcenter	(FHIA + FLOA) / 2
	BPFA.BWpass	(FHIA - FLOA)
	BPFA.BWstop	(FHIA - FLOA)
	All other ADS parameters are set to their default values.	

Notes

1. This component has been modeled as a subcircuit with two instances of BPF_Chebyshev.

Duplexer_E (Duplexer with Elliptic Filters)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *BPF Elliptic (Bandpass Filter, Elliptic)* (ccsys) in ADS.

GENESYS Symbol	ADS Component
DUPLEXER	genDuplexer_E
All other symbols	genDuplexer_E using the *Intermediate Subcircuit* (genlink) named genesyslib_Duplexer_E_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
FLOA		Used to calculate Fcenter and BWpass
FHIA		Used to calculate Fcenter and BWpass
FLOB		Used to calculate Fcenter and BWpass
FHIB		Used to calculate Fcenter and BWpass
NA	BPFA.N	
NB	BPFB.N	
RA	BPFA.Ripple	
RB	BPFB.Ripple	
ILA	BPFA.IL	
ILB	BPFB.IL	
SBAttn	BPFA.Astop, BPFB.Astop	
Amax	BPFA.MaxRej, BPFB.MaxRej	
Zin	S3P1.Z[1], BPFA.Z1, BPFB.Z1	
Zout	BPFA.Z2, BPFB.Z2	
	BPFA.Fcenter	(FHIA + FLOA) / 2
	BPFA.BWpass	(FHIA - FLOA)
	BPFA.BWstop	(FHIA - FLOA)
	All other ADS parameters are set to their default values.	

Notes

1. This component has been modeled as a subcircuit with two instances of BPF_Elliptic.

FREQ_MULT (RF Frequency Multiplier)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *Noisy2Port (Linear Noisy 2 Port Network)* (ccsrc) or *FreqMult (Ideal Frequency Multiplier)* (ccsys) in ADS.

GENESYS Symbol	ADS Component
FREQ_MULT	genFREQ_MULT
All other symbols	genFREQ_MULT using the *Intermediate Subcircuit* (genlink) named genesyslib_FREQ_MULT_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
CG		Used in FreqMult.G1 through FreqMult.G9.
MULT		Checked to be less than 10.
HL		Used in FreqMult.G1 through FreqMult.G9.
InDrv		Ignored.
RISO		FreqMult forces S12 to 0.
NOISE	Noisy2Port.NFMin	
ScaleBW		Ignored.
ZIN	FreqMult.Z1	
ZOUT	FreqMult.Z2	
	Noisy2Port.Rn = ZIN/4**(10^(NOISE/10) - 1)**	
	FreqMult.S11 = dbpolar(Min_dB,0)	See note 1.
	FreqMult.S22 = dbpolar(Min_dB,0)	See note 1.
	FreqMult.G1 = max(Min_dB,HL[1] + CG)	See note 2.
	FreqMult.G2 = max(Min_dB,HL[2] + CG)	See note 2.
	FreqMult.G3 = max(Min_dB,HL[3] + CG)	See note 2.
	FreqMult.G4 = max(Min_dB,HL[4] + CG)	See note 2.
	FreqMult.G5 = max(Min_dB,HL[5] + CG)	See note 2.
	FreqMult.G6 = max(Min_dB,HL[6] + CG)	See note 2.
	FreqMult.G7 = max(Min_dB,HL[7] + CG)	See note 2.
	FreqMult.G8 = max(Min_dB,HL[8] + CG)	See note 2.
	FreqMult.G9 = max(Min_dB,HL[9] + CG)	See note 2.
	FreqMult.Pmin = Min_dB	See note 1, 3.
	All other ADS parameters are set to their default values.	

Notes

1. Min_dB = -500.0 in dB
2. If the element of HL is available, otherwise ADS uses Min_dB.
3. InDrv could be mapped to Pmin for more realism, however, FREQ_MULT does not model InDrv.
4. genFREQ_MULT cannot be used in an S Parameter analysis.

HYBRID1 (Hybrid 90 Degree Coupler)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *S4P (4-Port S-parameter File)* (ccsim) in ADS.

GENESYS Symbol	ADS Component
HYBRID1	genHYBRID1
All other symbols	genHYBRID1 using the *Intermediate Subcircuit* (genlink) named genesyslib_HYBRID1_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
IL		See note 2.
CPL		See note 3.
ISO		See note 4.
GBAL		See note 6,8.
PBAL		See note 8.
ZIN1	S4P.Z[1]	
ZIN2	S4P.Z[2]	
ZIN3	S4P.Z[3]	
ZIN4	S4P.Z[4]	
	S12	See note 6,9.
	S13	See note 7,9.
	S14	See note 8,9.
	All other ADS parameters are set to their default values.	

Notes

1. This component has been modeled as a 4 port S parameter block, S4P.
2. IL_dB = -abs(IL)
3. CPL_dB = -abs(CPL)
4. ISO_dB = -abs(ISO)
5. MinS_lin = dbpolar(-300, 0)
6. S12 = dbpolar((IL_dB+CPL_dB+0.5*GBAL), 0)
7. S13 = dbpolar(ISO_dB, 0)
8. S14 = dbpolar(IL_dB + db(sqrt(1-dbpolar(2*CPL_dB, 0)))-0.5*GBAL), (-90-PBAL))
9. The S parameter block is set as follows:
    1. all port reflections are set to MinS_lin
    2. all port 1 to port 2 and port 3 to port 4 values are set to S12
    3. all port 1 to port 3 and port 2 to port 4 values are set to S13
    4. all port 1 to port 4 and port 2 to port 3 values are set to S14.

HYBRID180 (Hybrid 180 Degree Coupler)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *S4P (4-Port S-parameter File)* (ccsim) in ADS.

GENESYS Symbol	ADS Component
HYBRID180	genHYBRID180
All other symbols	genHYBRID180 using the *Intermediate Subcircuit* (genlink) named genesyslib_HYBRID180_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
IL		See note 2.
CPL		See note 3.
ISO		See note 4.
GBAL		See note 6,8.
PBAL		See note 8.
ZIN1	S4P.Z[1]	
ZIN2	S4P.Z[2]	
ZIN3	S4P.Z[3]	
ZIN4	S4P.Z[4]	
	S12	See note 6,9.
	S13	See note 7,9.
	S14	See note 8,9.
	All other ADS parameters are set to their default values.	

Notes

1. This component has been modeled as a 4 port S parameter block, S4P.
2. IL_dB = -abs(IL)

3. CPL_dB = -abs(CPL)
4. ISO_dB = -abs(ISO)
5. MinS_lin = dbpolar(-300, 0)
6. S12 = dbpolar((IL_dB+CPL_dB+0.5*GBAL), 0)
7. S13 = dbpolar(ISO_dB, 0)
8. S14 = dbpolar(IL_dB + db(sqrt(1-dbpolar(2*CPL_dB, 0)))-0.5*GBAL), (-180-PBAL))
9. The S parameter block is set as follows:
    1. all port reflections are set to MinS_lin
    2. all port 1 to port 2 and port 3 to port 4 values are set to S12
    3. all port 1 to port 3 and port 2 to port 4 values are set to S13
    4. all port 1 to port 4 and port 2 to port 3 values are set to S14.

ISO (Isolator)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *IsolatorSML (SMLIsolator)* (ccsys) in ADS.

GENESYS Symbol	ADS Component
ISO	IsolatorSML
All other symbols	IsolatorSML using the *Intermediate Subcircuit* (genlink) named genesyslib_ISO_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
IL	Loss1	
ISO	Isolate	
ZIN	Z1	
ZOUT	Z2	
	F1 = 0	
	F2 = 0	
	F3 = 0	
	VSWR = 1	
	CheckPassivity = no	
	All other ADS parameters are set to their default values.	

MIXER_BASIC

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *Mixer2 (RF System Mixer)* (ccsys) in ADS.

GENESYS Symbol	ADS Component
MIXER_RF	genMIXER_BASIC_RF
MIXER_IF	genMIXER_BASIC_IF
All other symbols	genMIXER_BASIC_RF using the *Intermediate Subcircuit* (genlink) named genesyslib_MIXER_RF_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
ConvGain		Used in Mixer2.ConvGain
SUM		Ignored.
LO		Ignored.
ISIDE		See note 1.
IR		See note 1.
NF	Mixer2.NF	
IP1dB		See note 2.
IPSAT		See note 2.
IIP3	Mixer2.TOI	
IIP2	Mixer2.SOI	
RTOI		Used in Mixer2.S21.
LTOR		Used in Mixer2.S13 and Mixer2.S31.
LTOI		Used in Mixer2.S23.
ZR	Mixer2.Z1	
ZI	Mixer2.Z2	
ZL	Mixer2.Z3	
InRevIso		Used in Mixer2.S12.
LORevIso		Used in Mixer2.S32.
	Mixer2.ConvGain = dbpolar(ConvGain,0)	
	Mixer2.RevConvGain = dbpolar(-300,0)	
	Mixer2.SP12 = dbpolar(-InRevIso,0)	
	Mixer2.SP13 = dbpolar(-LTOR,0)	
	Mixer2.SP21 = dbpolar(-RTOI,0)	
	Mixer2.SP23 = dbpolar(-LTOI,0)	
	Mixer2.SP31 = dbpolar(-LTOR,0)	
	Mixer2.SP32 = dbpolar(-LORevIso,0)	
	Mixer2.ReferToInput = INPUT	See note 3.
	All other ADS parameters are set to their default values.	

Notes

1. When image rejection is enabled in MIXER_BASIC, an image rejection mixer is modeled with image rejection applied at the input of two mixers. Image rejection in Mixer2 is used to suppress the intermodulation products of an image frequency at the output of a single mixer. The results can be so dissimilar that automatic mapping cannot be properly applied.
2. Both IP1dB and IPSAT are ignored, because Mixer2 cannot specify compression along with 2nd and 3rd order intercept parameters. Generating spectral lines at the proper frequencies is more important than calculating the correct power at these frequencies. This mapping will be sufficiently accurate for input power less than IP1dB.
3. Mixer2.SOI and Mixer2.TOI are referenced to the Mixer2 input port.

MIXER_DBAL (Double Balanced)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *Mixer2 (RF System Mixer)* (ccsys) in ADS.

GENESYS Symbol	ADS Component
MIXER_RF	genMIXER_DBAL_RF
MIXER_IF	genMIXER_DBAL_IF
All other symbols	genMIXER_DBAL_RF using the *Intermediate Subcircuit* (genlink) named genesyslib_MIXER_RF_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
ConvGain		Used in Mixer2.ConvGain
SUM		Ignored.
LO		Ignored.
ISIDE		See Note 1.
IR		See Note 1.
NF	Mixer2.NF	
ZR	Mixer2.Z1	
ZI	Mixer2.Z2	
ZL	Mixer2.Z3	
VF		See Note 7.
Alpha		See Note 4, 5.
Beta		See Note 4, 6.
Delta2		See Note 7.
Delta3		See Note 7.
Delta4		See Note 7.
IP1dB		See Note 2.
IPSAT		See Note 2.
InRevIso		Used in Mixer2.S12.
LORevIso		Used in Mixer2.S32.
	Mixer2.ConvGain = dbpolar(ConvGain,0)	
	Mixer2.RevConvGain = dbpolar(-300,0)	
	Mixer2.SP11 = dbpolar(Min_dB,0)	See Note 3.
	Mixer2.SP12 = dbpolar(-InRevIso,0)	
	Mixer2.SP13 = dbpolar(-LTOR_dB,0)	See Note 4.
	Mixer2.SP21 = dbpolar(-RTOI_dB,0)	See Note 5.
	Mixer2.SP22 = dbpolar(Min_dB,0)	See Note 3.
	Mixer2.SP23 = dbpolar(-LTOI_dB,0)	See Note 6.
	Mixer2.SP31 = dbpolar(-LTOR_dB,0)	See Note 4.
	Mixer2.SP32 = dbpolar(-LORevIso,0)	
	Mixer2.SP33 = dbpolar(Min_dB,0)	See Note 3.
	All other ADS parameters are set to their default values.	

Notes

1. When image rejection is enabled in MIXER_DBAL, an image rejection mixer is modeled with image rejection applied at the input of two mixers. In contrast, image rejection in Mixer2 is used to suppress the intermodulation products of an image frequency at the output of a single mixer. The results can be so dissimilar that automatic mapping cannot be properly applied.
2. Both IP1dB and IPSAT are ignored, because Mixer2 cannot specify compression along with 2nd and 3rd order intercept parameters. Generating spectral lines at the proper frequencies is more important than calculating the correct power at these frequencies. This mapping will be sufficiently accurate for input power less than IP1dB.
3. Min_dB = -316.948 in dB
4. LTOR_dB = LTOI_dB + RTOI_dB
5. RTOI_dB = max(db(min(max(1.0 - Alpha,0.0),1.0)),Min_dB)
6. LTOI_dB = max(db(min(max(1.0 - Beta,0.0),1.0)),Min_dB)
7. This parameter is normally used to calculate 3rd order and higher intermodulation powers, however, it cannot be used in this model.

PATH (Antenna (Path Loss))

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *Amplifier2 (RF System Amplifier)* (ccsys) in ADS.

GENESYS Symbol	ADS Component
PATH	genPATH
All other symbols	genPATH using the *Intermediate Subcircuit* (genlink) named genesyslib_PATH_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
G1		
G2		
Lossa		
Lossb		
DIST		
Loss1		
Loss2		
ZIN	Z1	
ZOUT	Z2	
	S11	dbpolar (0,0)
	S12	dbpolar (-1 **(abs(Lossb) + log10(DIST)** abs(Lossa) - (abs(G1) + abs(G2)) + abs(Loss1) + abs(Loss2)),0)
	S21	dbpolar (-1 **(abs(Lossb) + log10(DIST)** abs(Lossa) - (abs(G1) + abs(G2)) + abs(Loss1) + abs(Loss2)),0)
	S22	dbpolar (0,180)
	All other ADS parameters are set to their default values.	

PHASE (Phase Shifter)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *PhaseShiftSML (Phase Shifter)* (ccsys) in ADS.

GENESYS Symbol	ADS Component
PHASE_SHIFT	PhaseShiftSML
All other symbols	PhaseShiftSML using the *Intermediate Subcircuit* (genlink) named genesyslib_PHASE_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
A	Phase	
S	PhaseSlope	
F	FreqStart	
Z0	ZRef	
	RTConj = no	
	All other ADS parameters are set to their default values.	

PwrOscillator (Oscillator Power Source)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *P 1Tone (Power Source, Single Frequency)* (ccsrc) in ADS.

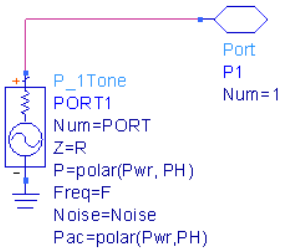
GENESYS Symbol	ADS Component
OSC	genPwrOscillator
All other symbols	genPwrOscillator using the *Intermediate Subcircuit* (genlink) named genesyslib_PwrOscillator_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
PORT	PORT	The genPwrOscillator component uses a P_1Tone component internally. PORT maps to Num of the P_1Tone component.
F	F	
Pwr	Pwr	
PH	PH	
EnablePN		Not mapped.
Foff		Not mapped.
PhaseN		Not mapped.
R	R	
	Noise = 1	
	All other ADS parameters are set to their default values.	

Notes

1. The ADS genPwrOscillator component is a subcircuit:



RFAMP (RF Amplifier (2nd - 3rd Order))

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *Amplifier2 (RF System Amplifier)* (ccsys) in ADS.

GENESYS Symbol	ADS Component
AMPL	genRFAMP
All other symbols	genRFAMP using the *Intermediate Subcircuit* (genlink) named genesyslib_RFAMP_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
G		Used in Amplifier2.S21.
NF	Amplifier2.NF	
OP1dB		See note 3.
OPSAT		See note 3.
OIP3	Amplifier2.TOI	
OIP2	Amplifier2.SOI	
RISO		Used in Amplifier2.S12.
FC		Used in Amplifier2.S21.
SLOPE		Used in Amplifier2.S21.
ZIN	Amplifier2.Z1	
ZOUT	Amplifier2.Z2	
	Amplifier2.S21 = dbpolar(max(G - SLOPE**ramp(log(max(freq,tinyreal)) - log(max(FC,tinyreal))),Min_dB),0)**	See note 1, 2.
	Amplifier2.S11 = dbpolar(Min_dB,0)	See note 1.
	Amplifier2.S22 = dbpolar(Min_dB,180)	See note 1.
	Amplifier2.S12 = dbpolar(-RISO,0)	
	All other ADS parameters are set to their default values.	

Notes

1. Min_dB = -317.0 in dB
2. freq is an simulation tool variable, and tinyreal is an AEL constant.
3. Both IP1dB and IPSAT are ignored, because Amplifier2 cannot specify compression along with 2nd and 3rd order intercept parameters. Generating spectral lines at the proper frequencies is more important than calculating the correct power at these frequencies. This mapping will be sufficiently accurate for input power less than IP1dB.

RFAMP_HO (RF Amplifier (High Order))

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *Amplifier2 (RF System Amplifier)* (ccsys) in ADS.

GENESYS Symbol	**ADS Component**
AMPL	genRFAMP_HO
All other symbols	genRFAMP_HO using the *Intermediate Subcircuit* (genlink) named genesyslib_RFAMP_HO_<SYMBOL>

Parameter Mapping

GENESYS	**ADS**	**Comments**
G		Used in Amplifier2.S21.
NF	Amplifier2.NF	
OP1dB		See note 3.
OPSAT		See note 3.
IMN		See note 5, 6, 7.
RISO		Used in Amplifier2.S12.
FC		Used in Amplifier2.S21.
SLOPE		Used in Amplifier2.S21.
ZIN	Amplifier2.Z1	
ZOUT	Amplifier2.Z2	
	Amplifier2.S21 = dbpolar(max(G - SLOPE**ramp(log(max(freq,tinyreal)) - log(max(FC,tinyreal))),Min_dB),0)**	See note 1, 2.
	Amplifier2.S11 = dbpolar(Min_dB,0)	See note 1.
	Amplifier2.S22 = dbpolar(Min_dB,180)	See note 1.
	Amplifier2.S12 = dbpolar(-RISO,0)	
	Amplifier2.SOI = SOI_Value	See note 6.
	Amplifier2.TOI - TOI_Value	See note 7.
	All other ADS parameters are set to their default values.	

Notes

1. Min_dB = -317.0 in dB
2. freq is an simulation tool variable, and tinyreal is an AEL constant.
3. Both IP1dB and IPSAT are ignored, because Amplifier2 cannot specify compression along with 2nd and 3rd order intercept parameters. Generating spectral lines at the proper frequencies is more important than calculating the correct power at these frequencies. This mapping will be sufficiently accurate for input power less than IP1dB.
4. MinIMN_dBm = -1000.0 dBm
5. IM1 = IMN[1], IM2 = IMN[2] and IM3 = IMN[3]. If an IMN element is not available, then MinIMN_dBm is used instead. Note that no intermodulation order higher than 3 is modeled.
6. SOI_Value = IM1 + (IM1 - IM2)/1
7. TOI_Value = IM1 + (IM1 - IM3)/2

S

SPLIT<n> (RF <n>-Way, 0 Degree Splitter/Combiner)

Documentation in this section is for translation information/notes only. For more

information, please see the GENESYS documentation for this model or refer to the documentation for *S1P Eqn to S6P Eqn (1- to 6-Port S-parameters, Equation-Based)* (ccsim) in ADS.

GENESYS Symbol	ADS Component
SPLIT<n>	genSPLIT<n>
All other symbols	genSPLIT<n> using the *Intermediate Subcircuit* (genlink) named genesyslib_SPLIT<n>_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
IL		
ISO	Isolation	
PH2.. PH		
GBal2.. GBal		
PH3		
Zin	Zref	
Zout		
	SP_Eqn.S	
	SP_Eqn.Z	
	All other ADS parameters are set to their default values.	

Notes

1. This component has been modeled as a 4 port S parameter block, S4P.
2. <n> is the number of output ports in a splitter.
3. S<n+1>P_Eqn.S is the scatter parameter matrix and has dimension (n+1,n+1) where 1 is the input, 2 is first output port and so on.
4. Z is the port impedance vector and has dimension (n+1). Z[1] is the input port impedance which is set to Zin. Z[2] is the output impedance of the first output port and so on.
5. The S parameter matrix is assigned as follows:
   S[j,i] = S[i,j]
   S[i,i] = dbpolar(-300,0)
   S[1,2]= dbpolar(- abs(IL),PH2)
   S[i,1] = dbpolar(- abs(IL)+GBal<i-1>,PH<i>)
   S[i,j] = dbpolar(- abs(ISO),0) when i!= j

SPLIT290 (RF 2-Way, 90 Degree Splitter/Combiner)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *S3P (3-Port S-parameter File)* (ccsim) in ADS.

GENESYS Symbol	ADS Component
SPLIT290	genSPLIT290
All other symbols	genSPLIT290 using the *Intermediate Subcircuit* (genlink) named genesyslib_SPLIT290_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
IL		See note 3.
ISO		See note 3.
PH2, PH3		See note 3,4.
GBal2		
Zin		See note 4.
Zout		See note 4.
	S3P_Eqn.S	See note 3.
	S3P_Eqn.Z	See note 4.
	All other ADS parameters are set to their default values.	

Notes

1. These components have been mapped to a custom ADS sub-circuit using the S3P_Eqn device.
2. S<n+1>P_Eqn.S is the scatter parameter matrix and has dimension (n+1,n+1) where 1 is the input, 2 is first output port and so on.
3. Z is the port impedance vector and has dimension (n+1). Z[1] is the input port impedance which is set to Zin. Z[2] and Z[3] are the output impedances and are set to Zout
4. The S parameter matrix is assigned as follows.
   S[j,i] = S[i,j]
   S[i,i] = dbpolar(-300,0)
   S[1,2]= dbpolar(- abs(IL),PH2)
   S[3,1] = dbpolar(- abs(IL)+GBal2,PH3)
   S[3,2] = dbpolar(- abs(ISO),0)

SPLIT2180 (RF 2-Way, 180 Degree Splitter/Combiner)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *S3P (3-Port S-parameter File)* (ccsim) in ADS.

GENESYS Symbol	ADS Component
SPLIT2180	genSPLIT2180
All other symbols	genSPLIT2180 using the *Intermediate Subcircuit* (genlink) named genesyslib_SPLIT2180_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
IL		See note 3.
ISO		See note 3.
PH2, PH3		See note 3,4.
GBal2		
Zin		See note 4.
Zout		See note 4.
	S3P_Eqn.S	See note 3.
	S3P_Eqn.Z	See note 4.
	All other ADS parameters are set to their default values.	

Notes

1. These components have been mapped to a custom ADS sub-circuit using the S3P_Eqn device.
2. S<n+1>P_Eqn.S is the scatter parameter matrix and has dimension (n+1,n+1) where 1 is the input, 2 is first output port and so on.
3. Z is the port impedance vector and has dimension (n+1). Z[1] is the input port impedance which is set to Zin. Z[2] and Z[3] are the output impedances and are set to Zout.
4. The S parameter matrix is assigned as follows.
   S[j,i] = S[i,j]
   S[i,i] = dbpolar(-300,0)
   S[1,2]= dbpolar(- abs(IL),PH2)
   S[3,1] = dbpolar(- abs(IL)+GBal2,PH3)
   S[3,2] = dbpolar(- abs(ISO),0)

SWITCH_Linear<n> (RF Switch)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *S1P (1-Port S-parameter File)* (ccsim)*S1P (1-Port S-parameter File)* (ccsim) in ADS.

GENESYS Symbol	ADS Component
SPST for n=1	genSWITCH_Linear<n>
All other symbols	genSWITCH_Linear<n> using the *Intermediate Subcircuit* (genlink) named genesyslib_SWITCH_Linear<n>_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
IL		See note 3.
ISO		See note 3.
State		See note 3, 4.
Zin		See note 4.
Zout		See note 4.
Zopen		See note 4.
	SP_Eqn.S	See note 3.
	SP_Eqn.Z	See note 4.
	All other ADS parameters are set to their default values.	

Notes

1. Min_dB = -317.0 in dB
2. n is the number of throws (outputs) in a switch. For this set of switches, n is between 1 and 20 inclusive. <n> takes integer values from 1 to n.
3. S is the scatter parameter matrix and has dimension (n+1,n+1) where 1 is the input, 2 is first throw (State=1), and so on until n+1 is the n-th throw (State=n). If State=p where p is from <n>, then (a) S[1,p+1] = S[p+1,1] = dbpolar(-IL, 0), (b) S[q,q] = dbpolar(Min_dB,0), and (c) all other elements of S is set to dbpolar(-ISO,0).
4. Z is the port impedance vector and has dimension (n+1). Z[1] is the input port impedance which is set to Zin. Z[2] is the output impedance of the first throw (State=1) and so on. If State=p where p is from <n>, then Z[p+1] has output impedance Zout with the rest of the throws having output impedance Zopen.

SWITCH_NonLinear<n> (RF Switch)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *S1P Eqn to S6P Eqn (1- to 6-Port S-parameters, Equation-Based)* (ccsim) and *Amplifier2 (RF System Amplifier)* (ccsys) in ADS.

GENESYS Symbol	ADS Component
SPST for n=1	genSWITCH_NonLinear<n>
All other symbols	genSWITCH_NonLinear<n> using the *Intermediate Subcircuit* (genlink) named genesyslib_SWITCH_NonLinear<n>_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
IL		See note 3.
ISO		See note 3.
State		See note 3, 4.
Zin		See note 4.
Zout		See note 4.
Zopen		See note 4.
IP1dB		See note 5.
IPSAT		See note 5.
IIP3		Used in Amplifier2.TOI.
IIP2		Used in Amplifier2.SOI.
	SP_Eqn.S	See note 3.
	SP_Eqn.Z	See note 4.
	Amplifier2.S21 = polar(1,0)	See note 6.
	Amplifier2.S11 = dbpolar(Min_dB,0)	See note 6.
	Amplifier2.S22 = dbpolar(Min_dB,0)	See note 6.
	Amplifier2.S12 = polar(1,0)	See note 6.
	Amplifier2.Z1 = SP_Eqn.Z[m+1]	See note 6.
	Amplifier2.Z2 = SP_Eqn.Z[m+1]	See note 6.
	Amplifier2.ReferToInput= INPUT	See note 6.
	Amplifier2.SOI = dbpolar(IIP2,0)	See note 6.
	Amplifier2.TOI = dbpolar(IIP3,0)	See note 6.
	All other ADS parameters are set to their default values.	

Notes

1. Min_dB = -317.0 in dB
2. n is the number of throws (outputs) in a switch. For this set of switches, n is between 1 and 20 inclusive. <n> takes integer values from 1 to n.
3. S is the scatter parameter matrix and has dimension (n+1,n+1) where 1 is the input, 2 is first throw (State=1), and so on until n+1 is the n-th throw (State=n). If State=p where p is from <n>, then (a) S[1,p+1] = S[p+1,1] = dbpolar(-IL, 0), (b) S[q,q] = dbpolar(Min_dB,0), and (c) all other elements of S is set to dbpolar(-ISO,0).
4. Z is the port impedance vector and has dimension (n+1). Z[1] is the input port impedance which is set to Zin. Z[2] is the output impedance of the first throw (State=1) and so on. If State=p where p is from <n>, then Z[p+1] has output impedance Zout with the rest of the throws having output impedance Zopen.
5. Both IP1dB and IPSAT are ignored, because Amplifier2 cannot specify compression along with 2nd and 3rd order intercept parameters. Generating spectral lines at the proper frequencies is more important than calculating the correct power at these frequencies. This mapping will be sufficiently accurate for input power less than IP1dB.
6. For n, <m> takes integer values from 1 to n-1.

T-Line

CPL (Coupled Lines)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *CLINP (Lossy Coupled Transmission Lines)* (ccdist) in ADS.

GENESYS Symbol	ADS Component
TRL_COUPLED	CLINP
All other symbols	CLINP using the *Intermediate Subcircuit* (genlink) named genesyslib_CPL_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
ZOE	Ze	
ZOO	Zo	
LENGTH	L	
KOE	Ke	
KOO	Ko	
AE	Ae	
AO	Ao	
F	F	
	All other ADS parameters are set to their default values.	

RCLIN (Distributed RC Transmission Line)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *RCLIN (Distributed R-C Network)* (ccdist) in ADS.

GENESYS Symbol	ADS Component
TLE	RCLIN
All other symbols	RCLIN using the *Intermediate Subcircuit* (genlink) named genesyslib_RCLIN_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
R	R	
C	C	
L	L	
	All other ADS parameters are set to their default values.	

TLE (Transmission Line)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *TLIN (Ideal 2-Terminal Transmission Line)* (ccdist) in ADS.

GENESYS Symbol	ADS Component
TLE	TLIN
All other symbols	TLIN using the *Intermediate Subcircuit* (genlink) named genesyslib_TLE_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
Z	Z	
L	E	
F	F	
A		Ignored.
	All other ADS parameters are set to their default values.	

TLE4 (Four-Terminal Transmission Line)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *TLIN4 (Ideal 4-Terminal Transmission Line)* (ccdist) in ADS.

GENESYS Symbol	ADS Component
TLE_FOUR	TLIN4
All other symbols	TLIN4 using the *Intermediate Subcircuit* (genlink) named genesyslib_TLE4_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
Z	Z	
L	E	
F	F	
A		Ignored.
	All other ADS parameters are set to their default values.	

TLP (Physical Transmission Line)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *TLINP (2-Terminal Physical Transmission Line)* (ccdist) in ADS.

GENESYS Symbol	ADS Component
TLE	TLINP
All other symbols	TLINP using the *Intermediate Subcircuit* (genlink) named genesyslib_TLP_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
Z	Z	
L	L	
K	K	
A	A	
F	F	
	TanD = 0	
	All other ADS parameters are set to their default values.	

TLP4 (Four-Terminal Transmission Line)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *TLINP4 (4-Terminal Physical Transmission Line)* (ccdist) in ADS.

GENESYS Symbol	ADS Component
TLE_FOUR	TLINP4
All other symbols	TLINP4 using the *Intermediate Subcircuit* (genlink) named genesyslib_TLP4_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
Z	Z	
L	E	
K	K	
A	A	
F	F	
	All other ADS parameters are set to their default values.	

Transistors

BIPNPN4 (Gummel-Poon BJT 4-Pin)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *M504 BJT4 NPN, M504 BJT4 PNP (Mextram 504 Nonlinear Bipolar Transistors with Substrate Terminal, NPN, PNP)* (ccnld) in ADS.

GENESYS Symbol	ADS Component
BIPNPN4	genBIPNPN4
All other symbols	genBIPNPN4 using the *Intermediate Subcircuit* (genlink) named genesyslib_BIPNPN4_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
Rbm	Rbm	See note 1
Lb		Not mapped
Lc		Not mapped
Le		Not mapped
	All other ADS parameters are set to their default values.	

Notes

1. The default value for Rbm in GENESYS is the value of Rb. In the ADS model, this parameter defaults to 0 and not the value of Rb.

BIPNPN (Gummel-Poon BJT)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *BJT NPN, BJT PNP (Bipolar Junction Transistors NPN, PNP)* (ccnld) in ADS.

GENESYS Symbol	ADS Component
BIPNPN	genBIPNPN
All other symbols	genBIPNPN using the *Intermediate Subcircuit* (genlink) named genesyslib_BIPNPN_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
Rbm	Rbm	See note 1
Lb		Not mapped
Lc		Not mapped
Le		Not mapped
	All other ADS parameters are set to their default values.	

Notes

1. The default value for Rbm in GENESYS is the value of Rb. In the ADS model, this parameter defaults to 0 and not the value of Rb.

BIPPNP4 (Gummel-Poon BJT 4-Pin)

Documentation in this section is for translation information/notes only. For more

information, please see the GENESYS documentation for this model or refer to the documentation for *M504 BJT4 NPN, M504 BJT4 PNP (Mextram 504 Nonlinear Bipolar Transistors with Substrate Terminal, NPN, PNP)* (ccnld) in ADS.

GENESYS Symbol	ADS Component
BIPPNP4	genBIPPNP4
All other symbols	genBIPPNP4 using the *Intermediate Subcircuit* (genlink) named genesyslib_BIPPNP4_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
Rbm	Rbm	See note 1
Lb		Not mapped
Lc		Not mapped
Le		Not mapped
	All other ADS parameters are set to their default values.	

Notes

1. The default value for Rbm in GENESYS is the value of Rb. In the ADS model, this parameter defaults to 0 and not the value of Rb.

BIPPNP (Gummel_Poon BJT)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *BJT NPN, BJT PNP (Bipolar Junction Transistors NPN, PNP)* (ccnld) in ADS.

GENESYS Symbol	ADS Component
BIPPNP	genBIPPNP
All other symbols	genBIPPNP using the *Intermediate Subcircuit* (genlink) named genesyslib_BIPPNP_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
Rbm	Rbm	See note 1
Lb		Not mapped
Lc		Not mapped
Le		Not mapped
	All other ADS parameters are set to their default values.	

Notes

1. The default value for Rbm in GENESYS is the value of Rb. In the ADS model, this parameter defaults to 0 and not the value of Rb.

BSIM3_N (BSIM3)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *BSIM3 Model (BSIM3 MOSFET Model)* (ccnld) in ADS.

GENESYS Symbol	ADS Component
N_FET	genBSIM3_N
All other symbols	genBSIM3_N using the *Intermediate Subcircuit* (genlink) named genesyslib_BSIM3_N_<SYMBOL>

Parameter Mapping

All GENESYS parameters are mapped to the corresponding ADS parameter. All other ADS parameters are set to their default values.

BSIM3_P (BSIM3)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *BSIM3 Model (BSIM3 MOSFET Model)* (ccnld) in ADS.

GENESYS Symbol	ADS Component
P_FET	genBSIM3_P
All other symbols	genBSIM3_P using the *Intermediate Subcircuit* (genlink) named genesyslib_BSIM3_P_<SYMBOL>

Parameter Mapping

All GENESYS parameters are mapped to the corresponding ADS parameter. All other ADS parameters are set to their default values.

CURTICE2_N (Curtice Quadratic)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *Curtice2 Model (Curtice-Quadratic GaAsFET Model)* (ccnld) in ADS.

GENESYS Symbol	ADS Component
N_FET	genCURTICE2_N
All other symbols	genCURTICE2_N using the *Intermediate Subcircuit* (genlink) named genesyslib_CURTICE2_N_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
M		Not mapped
	All other ADS parameters are set to their default values.	

CURTICE2_P (Curtice Quadratic)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *Curtice2 Model (Curtice-Quadratic GaAsFET Model)* (ccnld) in ADS.

GENESYS Symbol	ADS Component
P_FET	genCURTICE2_P
All other symbols	genCURTICE2_P using the *Intermediate Subcircuit* (genlink) named genesyslib_CURTICE2_P_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
M		Not mapped
	All other ADS parameters are set to their default values.	

CURTICE3_N (Curtice Cubic)

Documentation in this section is for translation information/notes only. For more

information, please see the GENESYS documentation for this model or refer to the documentation for *Curtice3 Model (Curtice-Cubic GaAsFET Model)* (ccnld) in ADS.

GENESYS Symbol	ADS Component
N_FET	genCURTICE3_N
All other symbols	genCURTICE3_N using the *Intermediate Subcircuit* (genlink) named genesyslib_CURTICE3_N_<SYMBOL>

Parameter Mapping

All GENESYS parameters are mapped to the corresponding ADS parameter. All other ADS parameters are set to their default values.

CURTICE3_P (Curtice Cubic)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *Curtice3 Model (Curtice-Cubic GaAsFET Model)* (ccnld) in ADS.

GENESYS Symbol	ADS Component
P_FET	genCURTICE3_P
All other symbols	genCURTICE3_P using the *Intermediate Subcircuit* (genlink) named genesyslib_CURTICE3_P_<SYMBOL>

Parameter Mapping

All GENESYS parameters are mapped to the corresponding ADS parameter. All other ADS parameters are set to their default values.

STATZ_N (Curtice Quadratic)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *Statz Model (Statz Raytheon GaAsFET Model)* (ccnld) in ADS.

GENESYS Symbol	ADS Component
N_FET	genSTATZ_N
All other symbols	genSTATZ_N using the *Intermediate Subcircuit* (genlink) named genesyslib_STATZ_N_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
M		Not mapped
R1		Not mapped
R2		Not mapped
RC		Not mapped
RF		Not mapped
TRD1		Not mapped
TRG1		Not mapped
TRS1		Not mapped
	All other ADS parameters are set to their default values.	

STATZ_P (Curtice Quadratic)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *Statz Model (Statz Raytheon GaAsFET Model)* (ccnld) in ADS.

GENESYS Symbol	ADS Component
P_FET	genSTATZ_P
All other symbols	genSTATZ_P using the *Intermediate Subcircuit* (genlink) named genesyslib_STATZ_P_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
M		Not mapped
R1		Not mapped
R2		Not mapped
RC		Not mapped
RF		Not mapped
TRD1		Not mapped
TRG1		Not mapped
TRS1		Not mapped
	All other ADS parameters are set to their default values.	

TOM3_N (Tom3 Verilog_A model)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *TOM3 Model (TriQuint TOM3 Scalable Nonlinear FET Model)* (ccnld) in ADS.

GENESYS Symbol	ADS Component
N_FET	genTOM3_N
All other symbols	genTOM3_N using the *Intermediate Subcircuit* (genlink) named genesyslib_TOM3_N_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
Delta		Not mapped
Vdelta		Not mapped
M		Not mapped
N		Not mapped
Noise		Not mapped
	All other ADS parameters are set to their default values.	

TOM3_P (Tom3 Verilog_A model)

Documentation in this section is for translation information/notes only. For more information, please see the GENESYS documentation for this model or refer to the documentation for *TOM3 Model (TriQuint TOM3 Scalable Nonlinear FET Model)* (ccnld) in ADS.

GENESYS Symbol	ADS Component
P_FET	genTOM3_P
All other symbols	genTOM3_P using the *Intermediate Subcircuit* (genlink) named genesyslib_TOM3_P_<SYMBOL>

Parameter Mapping

GENESYS	ADS	Comments
Delta		Not mapped
Vdelta		Not mapped
M		Not mapped
N		Not mapped
Noise		Not mapped
	All other ADS parameters are set to their default values.	

Substrate Translation

The following section details translation information for substrate translation.

Mapping ADS Substrates

The following table details the transmission line technologies currently supported by the ADS link.

Transmission Line Technologies	Supported by the ADS Link
Ideal	yes
Microstrip (Standard)	yes
Stripline (Standard)	yes
Stripline (Offset)	yes
Coax	no
Square Coax (Square Conductor)	no
Square Coax (Round Conductor)	no
Coplanar	no
Coplanar with Ground	no
Microstrip (Inverted)	no
Microstrip (Suspended)	no
Slabline (Round Rod)	no

MSUB (Microstrip Substrate)Substrate Mapping

ADS	GENESYS	Comments
H	Height	
Er	Er	
Mur		Not mapped. GENESYS assumes Mur = 1
Cond	Rho = 1/(Cond*1.724e-8)	
Hu		Not specified on GENESYS substrate
T	Thick	
TanD	Tand	
Rough	Sr	

SSUB (Stripline Substrate)Substrate Mapping

ADS	GENESYS	Comments
Er	Er	
Mur		Not mapped. GENESYS assumes Mur = 1
B	Height	
T	Thick	
Cond	Rho = 1/(Cond*1.724e-8)	
TanD	Tand	
	Sr = 0	

SSSUB (Suspended Substrate) Substrate Mapping

ADS	GENESYS	Comments
H	Height	
Er	Er	
Mur		Not mapped. GENESYS assumes Mur = 1
Cond	Rho = 1/(Cond*1.724e-8)	
Hu		Not a substrate parameter.
H1		Not a substrate parameter.
T	Thick	
TanD	Tand	

CPWSUB (Coplanar Waveguide Substrate) Substrate Mapping

ADS	GENESYS	Comments
H	Height	
Er	Er	
Mur		Not mapped. GENESYS assumes Mur = 1
Cond	Rho = 1/(Cond*1.724e-8)	
T	Thick	
TanD	Tand	
Rough	Sr	

PCSUB1 (PCB Substrate) Substrate Mapping

ADS	GENESYS	Comments
H[1]	Height	
Er	Er	
Cond	Rho = 1/(Cond*1.724e-8)	
Hu		Not a substrate parameter.
H1		Not a substrate parameter.
T	Thick	
W		Not a substrate parameter.
Sigma		Not a substrate parameter.
TanD	Tand	

MLSUBSTRATE2 (Multilayer Substrate, 2 Layers) Substrate Mapping

ADS	GENESYS	Comments
Er	Er	
H	Height	
TanD	Tand	
T[1]	Thick	
Cond[1]	Rho = 1/(Cond*1.724e-8)	
T[2]		Not a substrate parameter.
Cond[2]		Not a substrate parameter.

Non-Mapped Substrates

The following table lists ADS substrates with no GENESYS counterpart.

ADS Substrate Name	Description
FSUB	Finline substrate
MLSUBSTRATE3	Multi-layer substrate, 3 layers
MLSUBSTRATE4	Multi-layer substrate, 4 layers
MLSUBSTRATE5	Multi-layer substrate, 5 layers
MLSUBSTRATE6	Multi-layer substrate, 6 layers
MLSUBSTRATE7	Multi-layer substrate, 7 layers
MLSUBSTRATE8	Multi-layer substrate, 8 layers
MLSUBSTRATE9	Multi-layer substrate, 9 layers
MLSUBSTRATE10	Multi-layer substrate, 10 layers
MLSUBSTRATE12	Multi-layer substrate, 12 layers
MLSUBSTRATE14	Multi-layer substrate, 14 layers
MLSUBSTRATE16	Multi-layer substrate, 16 layers
MLSUBSTRATE32	Multi-layer substrate, 32 layers
MLSUBSTRATE40	Multi-layer substrate, 40 layers
MSUBST3	Microstrip 3-layer substrate
PCSUB2	2-layer printed circuit substrate
PCSUB3	3-layer printed circuit substrate
PCSUB4	4-layer printed circuit substrate
PCSUB5	5-layer printed circuit substrate
PCSUB6	6-layer printed circuit substrate
PCSUB7	7-layer printed circuit substrate
SSSUBO	Offset stripline substrate

Mapping GENESYS Substrates

When a GENESYS schematic is exported to ADS, a substrate is inserted onto the ADS schematic if any component needs it. The ADS substrates supported during schematic export are:

- CPWSUB - Coplanar waveguide
- MSUB - Microstrip
- MLSUBTRATE2 - Multi-layer substrate
- SSUB - Stripline
  The substrate parameters are mapped as follows:

GENESYS substrate mapped to MSUB (Microstrip substrate) Substrate Mapping

GENESYS substrate parameter	ADS MSUB parameter	Comments
Er	Er	
Tand	TanD	
Rho	Cond = 1/(Rho*1.724e-8)	Rho is resistivity relative to annealed copper. Cond is conductivity in Siemens/m
Thick	T	
Sr	Rough	
Height	H	
LibName		Not mapped.
	All other ADS parameters are set to their default values.	

GENESYS substrate mapped to SSUB (Stripline substrate) Substrate Mapping

GENESYS substrate parameter	ADS MSUB parameter	Comments
Er	Er	
Tand	TanD	
Rho	Cond = 1/(Rho*1.724e-8)	Rho is resistivity relative to annealed copper. Cond is conductivity in Siemens/m
Thick	T	
Sr		Not mapped.
Height	B	
LibName		Not mapped.
	All other ADS parameters are set to their default values.	

GENESYS substrate mapped to CPWSUB (Coplanar waveguide substrate) Substrate Mapping

GENESYS substrate parameter	ADS MSUB parameter	Comments
Er	Er	
Tand	TanD	
Rho	Cond = 1/(Rho*1.724e-8)	Rho is resistivity relative to annealed copper. Cond is conductivity in Siemens/m
Thick	T	
Sr	Rough	
Height	H	
LibName		Not mapped.
	All other ADS parameters are set to their default values.	

GENESYS substrate mapped to MLSUBSTRATE2 (Multi-layer substrate) Substrate Mapping

GENESYS substrate parameter	ADS MSUB parameter	Comments
Er	Er	
Tand	TanD	
Rho	Cond[1] = 1/(Rho*1.724e-8) Cond[2] = 1/(Rho*1.724e-8)	Rho is resistivity relative to annealed copper. Cond is conductivity in Siemens/m
Thick	T[1] T[2]	
Sr		Not mapped.
Height	H	
LibName		Not mapped.
	All other ADS parameters are set to their default values.	

Troubleshooting GENESYS Synthesis-SPECTRASYS Link

This section offers troubleshooting tips, and discusses error, warning messages and known issues.

Blank Spot on ADS Schematic

Issue

Blank spot on an ADS schematic that has been imported from GENESYS.

Solution

A non-exisitent mapping is present, see *Non-Existent Mappings* (genlink) more information.

DisCos Do Not Transfer

Issue

In addition to the regular discontinuity symbols, GENESYS provides a set of small, single-node symbols called "DisCos". DisCos are special symbols used by GENESYS to make drawing circuits more convenient. They are small circles with a picture of a discontinuity that are placed on top of a single node. These symbols do not transfer well to ADS.

Solution

You should always use standard discontinuities if you will be exporting your circuit to ADS.

Note
This does *not* affect simulation results in GENESYS: Standard Discontinuities and Discos give identical simulation results.

Error Message on Simulation

Issue:

Error message when you simulate.

```
Error detected by hpeesofsim during netlist parsing.
illegal: valid characters in design names are alphanumeric or _`@#&+-=^
Instance `InstanceName' in design `\WorkspaceName\networks\DesignName' is
a non-simulatable data-based model. It is a placeholder for a GENESYS
component that could not be transferred to ADS.
```

Solution:

The schematic you are simulating contains a non-simulatable component. There are several SPECTRASYS components that have no counterpart in ADS. These components are transferred into ADS as non-simulatable components. To perform a simulation in ADS, you need to replace each instance of a non-simulatable component with an instance of a regular ADS component or with an instance of a subcircuit that you create to model the component. See *Non-Simulatable Components* (genlink) for more information.

genesyslib Components

Issue:

genesyslib components on your ADS schematic.

Solution:

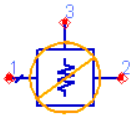
These are intermediate subcircuits. They are created during the schematic transfer whenever the symbol used by a GENESYS instance does not match the ADS symbol for the corresponding ADS component. See *Intermediate Subcircuit* (genlink) for more information.

Note
GENESYS has a symbol library named SymbolsQtr that contains symbols that are compatible with ADS symbols. To get GENESYS to use this library when inserting parts, set the "Use 1/4 grid symbols" checkbox on the Schematic tab of the GENESYS Options dialog box. If GENESYS is launched from ADS, this option is set automatically.

Non-Simulatable Components

Issue:

Components with orange circle-slashes through them.



Solution:

There are several SPECTRASYS components that have no counterpart in ADS. These components are transferred into ADS as non-simulatable components. To perform a simulation in ADS, you need to replace each instance of a non-simulatable component with an instance of a regular ADS component or with an instance of a subcircuit that you create to model the component. See *Non-Simulatable Components* (genlink) for more information.

TestBench Schematics

Issue:

Not sure what the TestBench Schematics are used for.

Solution:

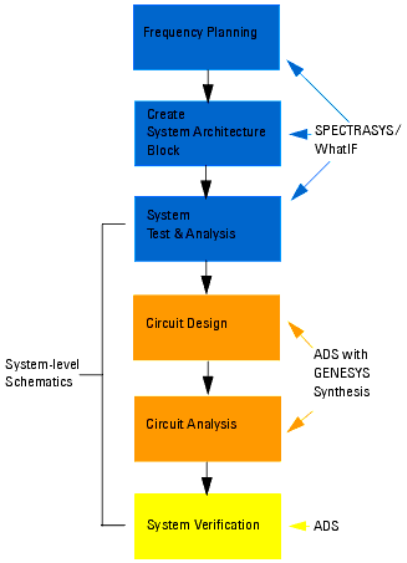
The TestBench schematic named DesignName_TestBench lets you simulate the S-parameters of the design DesignName. When you transfer designs from GENESYS to ADS, you have the option of transferring S-Parameter simulation control components, too. When this option is selected, the link creates a TestBench design in ADS for each GENESYS schematic that has a GENESYS Linear Analysis associated with it. TestBenches are created only for S-Parameter simulations. Other simulation types (e.g., harmonic balance, transient, optimization) are not transferred. See the *Exporting TestBenches* (genlink) for more information.

Using the GENESYS Synthesis/SPECTRASYS link from ADS

This section details how to use the GENESYS Synthesis/SPECTRASYS link from ADS.

GENESYS Synthesis/SPECTRASYS Design Flow

The following illustration shows the flow of engineering tasks and how GENESYS Synthesis, SPECTRASYS, and ADS take part.



How the GENESYS Synthesis/SPECTRASYS link works

The link between ADS and GENESYS Synthesis/SPECTRASYS allows you to transfer GENESYS schematics to ADS. It is available only from Windows installations. GENESYS is not available in UNIX. The link transfers only schematics and linear simulations. It does not transfer layouts, plots, or datasets.

To transfer a schematic from GENESYS to ADS, both GENESYS and ADS must be running. In GENESYS, the Workspace that contains the schematic must be open. In ADS, the workspace to which the schematic will be transferred must be open.

Note
The link transfers schematics only from GENESYS to ADS. It does not transfer schematics from ADS to GENESYS.

Establishing the link

To establish a link between ADS and GENESYS, you can Launch GENESYS from ADS. This automatically establishes a link between the current ADS workspace and the GENESYS Workspace. Select the *File* > *Export* > *Export Schematic to ADS* command in GENESYS. See Transferring schematics from GENESYS to ADS for more information.

Breaking the link

The run-time link connects an open ADS workspace and an open GENESYS Workspace.

The link is broken when: You close the current workspace in ADS, by either closing the workspace itself or exiting ADS. You close the current Workspace in GENESYS, by either closing the Workspace itself or by exiting GENESYS.

Folders used by the GENESYS Synthesis/SPECTRASYS link

The ADS workspace folder

When you launch GENESYS from ADS, the default folder for saving the GENESYS workspace is in the ADS workspace. The advantage of this is that when you archive the ADS workspace, the GENESYS workspace get included in the archive.
The workspace for synthesis is saved in the folder

MyWorkspace_wrk\workspaces\synthesis

The workspace for SPECTRASYS is saved in the folder

MyWorkspace_wrk\workspaces\spectrasys

If these folders do not exist, ADS creates them as needed.

The Temp directory

When exporting schematics to ADS, GENESYS creates two files. Transfer.iff is the IFF file that is used to transfer the schematics from GENESYS to ADS. Transfer.log is a log file that contains messages generated during the export.

These files are located in the Temp folder that is based on your Windows user name:

C:\Documents and Settings\userName\Local Settings\Temp

Where `userName` is your Windows user name.

Component Mappings

An instance on a GENESYS schematic has two important pieces of information, the model and the symbol. The Model determines what parameters the instance has and how the instance is simulated. An instance that uses the RES model has one parameter, named R, and simulates as a two-terminal ideal resistor. An instance that uses an IND model has one parameter, named L, and simulates as a two-terminal ideal inductor. The Symbol determines how the instance is drawn on the schematic. An instance that has the RESISTOR symbol is drawn as a two-terminal resistor. An instance with the INDUCTOR symbol is drawn as a two-terminal inductor.

After you insert an instance on a GENESYS schematic, you can change its symbol without changing its model. This is quite different from ADS. In ADS, a component has a fixed simulation model and a fixed symbol. When you insert an instance of a component in ADS, you cannot change its symbol.

When GENESYS transfers an instance to ADS, GENESYS looks for the component mapping that corresponds to the model/symbol pair of the GENESYS instance. That mapping, if it exists, tells GENESYS which ADS component to use. It also tells GENESYS how to map the GENESYS model parameters to the ADS component parameters.

Example 1:

A GENESYS instance for a resistor has Model=RES and Symbol=RESISTOR. The parameter R is set to 50. This is a standard model/symbol pair and the component mapping exists. The mapping, see *RES (Ideal Resistor)* (genlink), indicates that the corresponding ADS component is R. It also specifies that the R parameter of the GENESYS RES model corresponds directly to the R parameter of the ADS R component. GENESYS transfers the instance as an instance of the R ADS component. It sets the value of the ADS instance's R parameter to 50.

A GENESYS instance can use a user-defined symbol that the mapping rules know nothing about. Or the GENESYS instance can use a non-standard symbol (such as using the INDUCTOR symbol with the RES model). To map this instance to an ADS component, an intermediate subcircuit is used.

Intermediate Subcircuit

When GENESYS finds a component mapping that matches the GENESYS model but cannot find a component mapping that matches both the GENESYS model and symbol, GENESYS creates a new ADS subcircuit. We call this an *intermediate* subcircuit. Its sole purpose is to provide a new symbol for an ADS component.

You can recognize an intermediate subcircuit by its component name. It always starts with *genesyslib* .

The symbol for the intermediate subcircuit is a copy of the GENESYS symbol. The

schematic for the subcircuit contains exactly one instance. It's an instance of the ADS component that corresponds to the GENESYS model. The name of the intermediate subcircuit is genesyslib<MODEL><SYMBOL>, where MODEL is replaced by the GENESYS model name and SYMBOL is replaced by the GENESYS symbol name. The parameters of the intermediate subcircuit are the same as the parameters of the GENESYS model. The parameters of the ADS instance inside the subcircuit are set to the corresponding parameters of the subcircuit.

Example 2:

A GENESYS instance for a resistor has Model=RES and Symbol=MyResistor where MyResistor is a user-defined symbol. The parameter R is set to 50. This is not a standard model/symbol pair and no mapping exists that matches both the model and the symbol. But a mapping is found that matches the model. (This is the same mapping found in example 1.) The mapping indicates that the ADS R component corresponds to the RES model, see *RES (Ideal Resistor)* (genlink). It also specifies that the R parameter of the GENESYS RES model corresponds directly to the R parameter of the ADS R component. GENESYS creates a two-terminal ADS subcircuit called genesyslib_RES_MyResistor. The symbol for this ADS subcircuit is a copy of the MyResistor symbol. The schematic for this subcircuit is an instance of an R component with each pin connected to a port of the subcircuit. The subcircuit has one parameter R. The R parameter of the ADS R component inside the subcircuit is set to R. You can see that this subcircuit simulates exactly like the ADS R component. Its only purpose is to provide a different symbol.

Caution
Do not modify intermediate subcircuits. They can be overwritten, without warning, any time you transfer a GENESYS schematic into your ADS workspace.

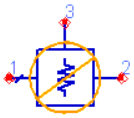
Non-Existent Mappings

Sometimes there is no mapping found for a particular GENESYS model. This happens for a variety of reasons: Vendor library parts for which there are no mapping rules. User-defined Verilog-A models for which there are no mapping rules.* Standard models that don't have a corresponding ADS component.* Standard models for which we have not yet created a mapping rule.

When no mapping rule is found, GENESYS emits an error. The schematic transfer continues, leaving a blank spot in the ADS schematic where the component should be. Pay attention to these error messages. In most cases, the ADS schematic will still simulate even with missing instances. Most of the time, if you do simulate, the results will be unrealistic, signaling a problem. There can be cases where the simulation results appear somewhat reasonable even though the circuit is incomplete.

Non-Simulatable Components

To reduce the potential confusion of simulating circuits that have missing components, non-simulatable components are used. A *non-simulatable* component is an ADS component that will generate an error upon simulation in ADS. The symbol for a non-simulatable component looks like a normal ADS symbol, but it has an orange circle/slash symbol to indicate that it's non-simulatable.



If you do try to simulate, an error message will appear in the Status Server:

Error detected by hpeesofsim during netlist parsing.
illegal: valid characters in design names are alphanumeric or _`@#&+-=^
Instance `InstanceName' in design `\WorkspaceName\networks\DesignName' is a non-simulatable data-based model. It is a placeholder for a GENESYS component that could not be transferred to ADS.

To perform a simulation in ADS, you need to replace each instance of a non-simulatable component with an instance of a regular ADS component or with an instance of a subcircuit that you create to model the component.

For a comprehensive list, see *Non-Simulatable Components* (genlink) in the Model Translation section.

Exporting TestBenches

When you export schematics from GENESYS to ADS, you have the option of exporting TestBenches. When this option is selected, GENESYS exports a TestBench schematic for every exported GENESYS schematic that has a GENESYS Linear simulation associated with it.

For instance, when you export a schematic named `MySchematic` and there is a linear simulation in GENESYS for `MySchematic` , then the exporter exports two schematics to ADS. One is `MySchematic` , and the other is `MySchematic_TestBench` . The testbench schematic is used to calculate the S-parameters of `MySchematic` . It contains an instance of `MySchematic` , Term components to terminate the instance, and an S-Parameter simulation controller with settings derived from the GENESYS Linear simulation.

Caution
Changes to a TestBench schematic in ADS will be overwritten if you re-export the TestBench schematic. To avoid overwriting changes, do not re-export TestBenches.

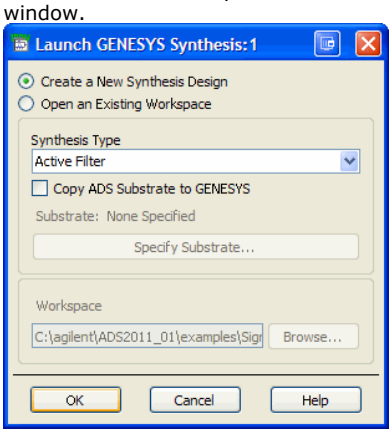
Benefit of using TestBenches

An ADS schematic can contain both circuitry and simulation control, so why use TestBenches for simulation control? Separating the simulation schematic from the circuit schematic makes the circuit schematic immediately reusable. If the simulation control components were placed on the circuit schematic, then the circuit schematic could not be used as a subcircuit without first deactivating the simulation components and the Term components.

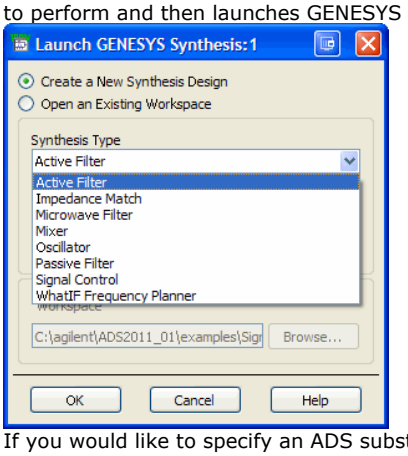
Note
Only linear simulations are exported from GENESYS. Other simulation types (harmonic balance, transient, optimization, etc.) are not exported.

Using GENESYS Synthesis from ADS

To launch GENESYS Synthesis select Tools > GENESYS Synthesis from the schematic window.



You need to specify whether you want to create a new design or open an existing Workspace. If creating a new Synthesis design, ADS asks what type of synthesis you'd like to perform and then launches GENESYS preconfigured to perform the synthesis.



If you would like to specify an ADS substrate to copy, select the checkbox, then click the

Specify Substrate button.

The Select Substrate dialog will appear. Specify which substrate you would like to copy and click *OK* . You should now see the name of the selected substrate appear in the *Launch GENESYS Synthesis* dialog, click *OK* .

GENESYS will start a new design while ADS runs in a separate window. When you are finished, refer to Transferring schematics from GENESYS to ADS.

Note
See GENESYS documentation for information on how to create/manipulate information in GENESYS.

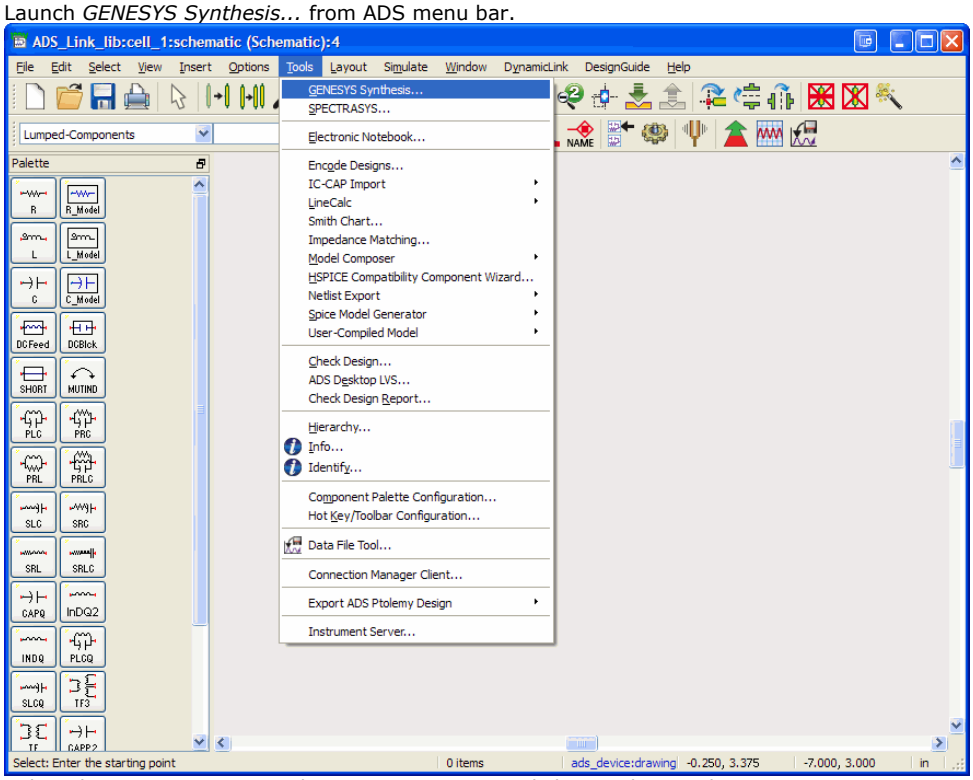
Accessing EQUALIZE and S/FILTER

EQUALIZE and S/FILTER are compatible with ADS. However, they are not accessible from the ADS synthesis menu. To use them, start GENESYS by launching SPECTRASYS with a blank schematic. Once you are in GENESYS, follow the tutorials for these programs in the GENESYS online help. When you are done synthesizing your circuits, you should save your files and export to ADS using the *File > Export > Export Schematic to ADS* command in GENESYS.

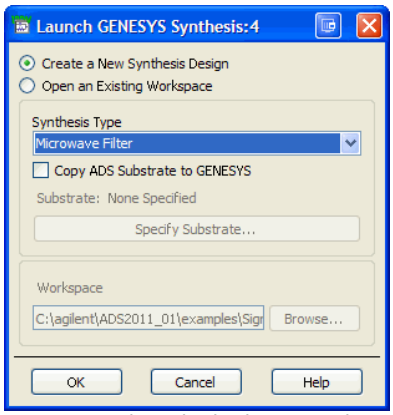
Example using the GENESYS Synthesis link

The following section details how to design a Butterworth low pass filter using the GENESYS Synthesis Link.

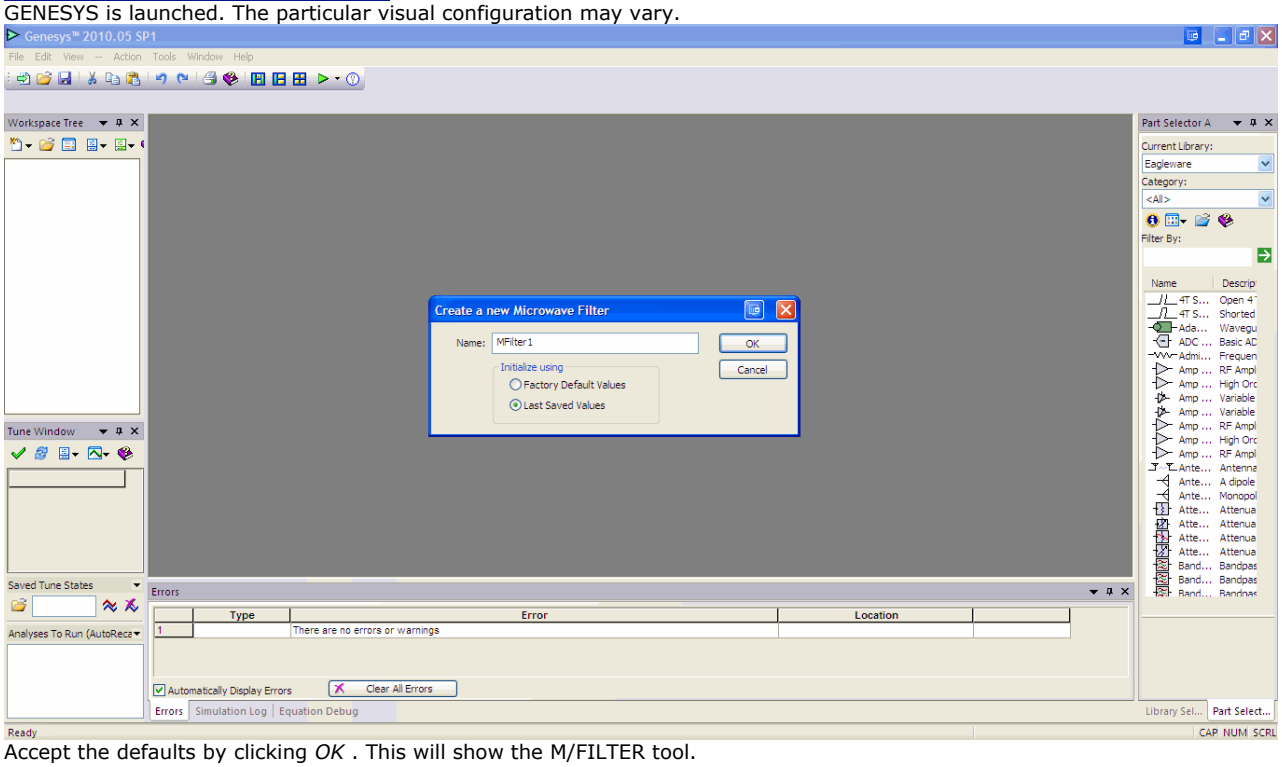
1. Launch *GENESYS Synthesis...* from ADS menu bar.



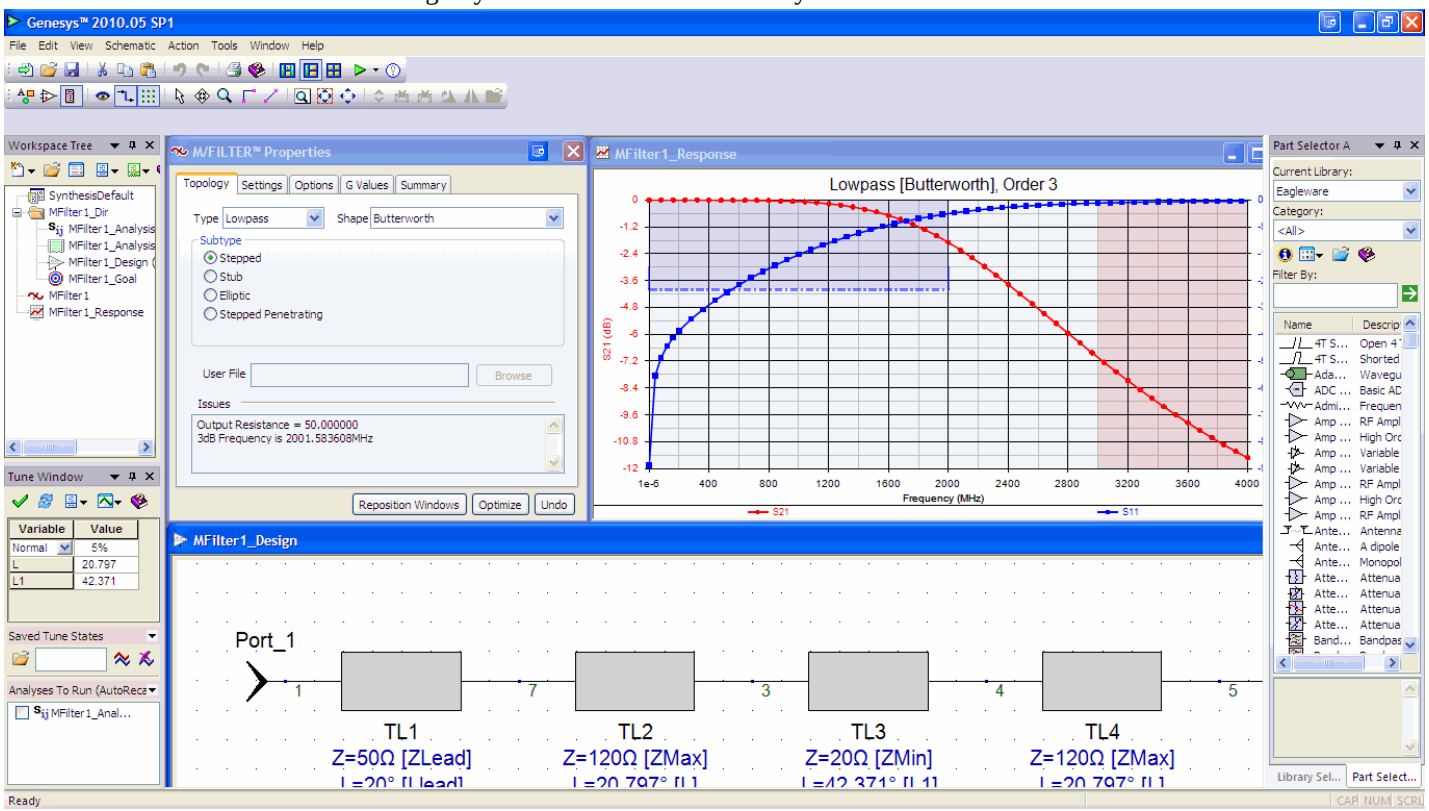
2. Select the *Create a New Synthesis Design* option and change the *Synthesis Type* to Microwave Filter. If required, the substrate can be defined with GENESYS. However, an ADS substrate can be used by checking the *Copy ADS Substrate to GENESYS* box.



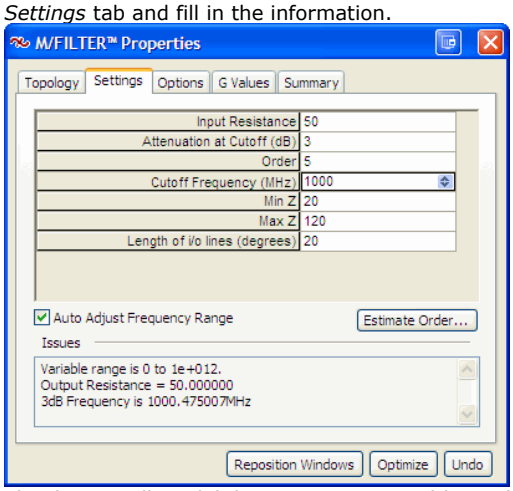
3. GENESYS is launched. The particular visual configuration may vary.



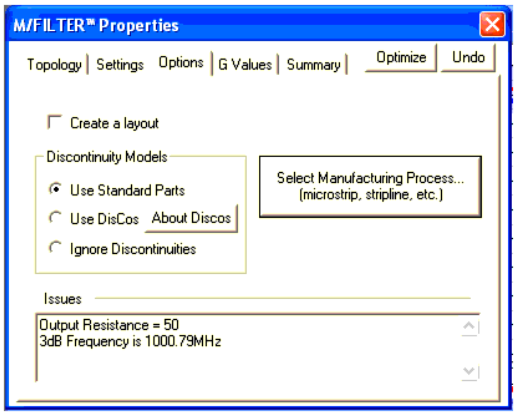
4. Accept the defaults by clicking *OK* . This will show the M/FILTER tool.
5. We are designing a low pass Butterworth filter, so select Butterworth from the *Shape* drop-down. Lowpass will be the default under *Type* . *Subtype* refers to the particular architecture that will implement the filter. The list of subtypes will vary with Type and Shape.



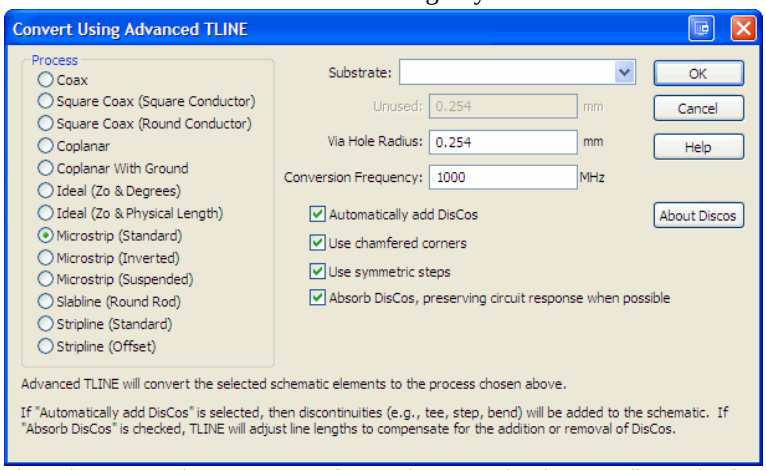
6. Our filter will be of the order 5, and have a cutoff frequency at 1 GHz. Select the *Settings* tab and fill in the information.



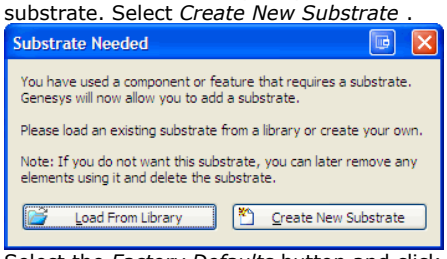
7. The design will model discontinuities in widths. Select the *Options* tab, and click the *Select Manufacturing Process...* button.



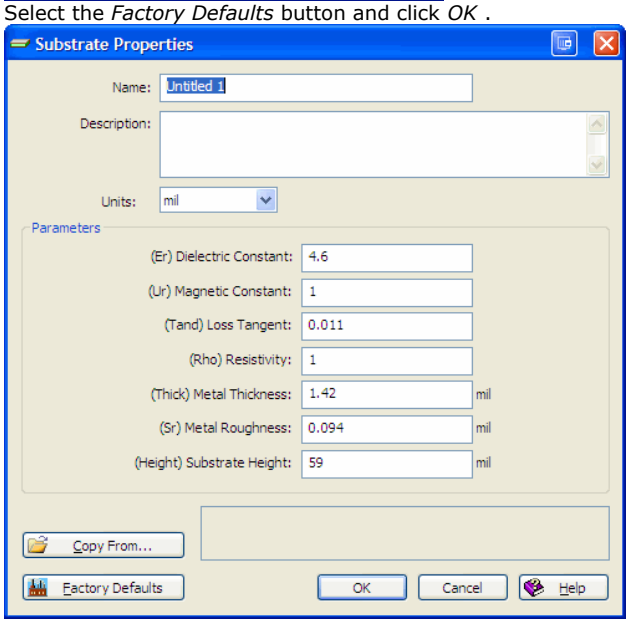
8. We choose to design our filter with standard microstrips.



9. The M/FILTER tool now prompts for a substrate. The design will use the factory substrate. Select *Create New Substrate* .



10. Select the *Factory Defaults* button and click *OK* .

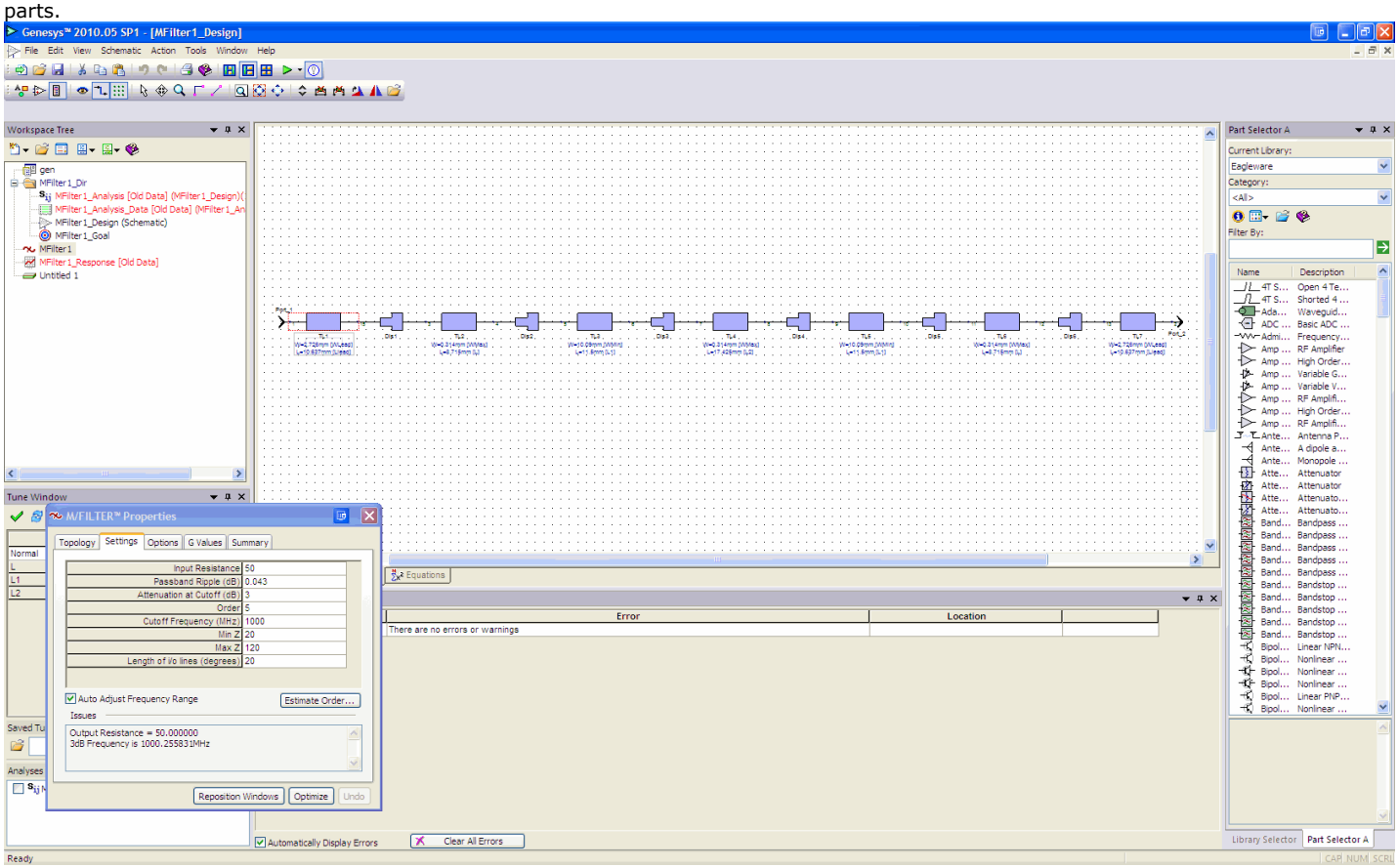


11. We look at the summary tab and then press the *Optimize* button for design refinement.

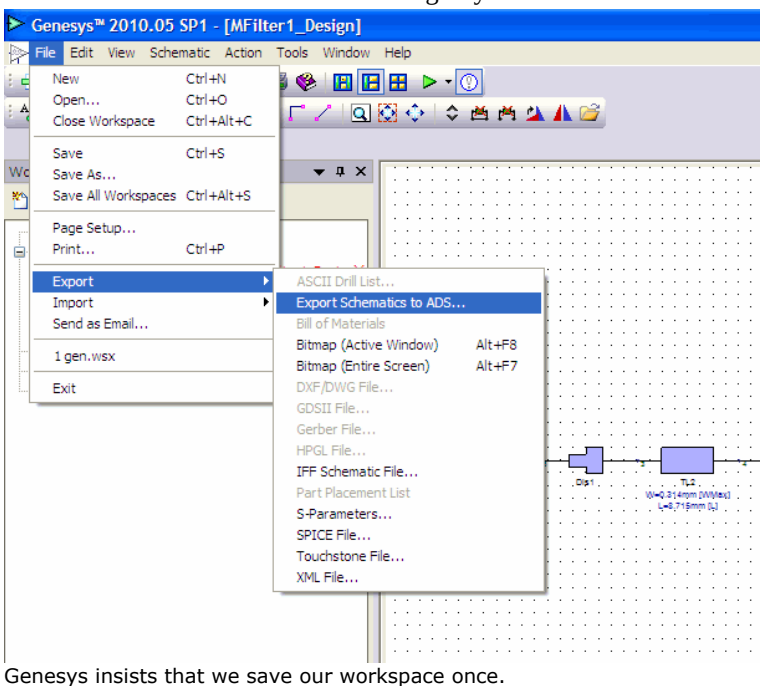
12. After 500 iterations or so, we stop our optimization. We check the S11 and S12

characterization of our design.

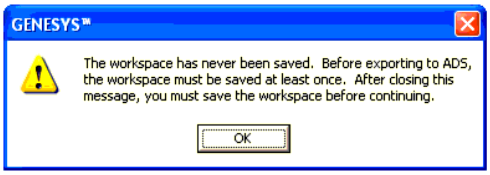
13. The design schematic shows a sequence of microstrip lines of varying length and width, in a straight line. Between the microstrip lines are discontinuity modeling parts.



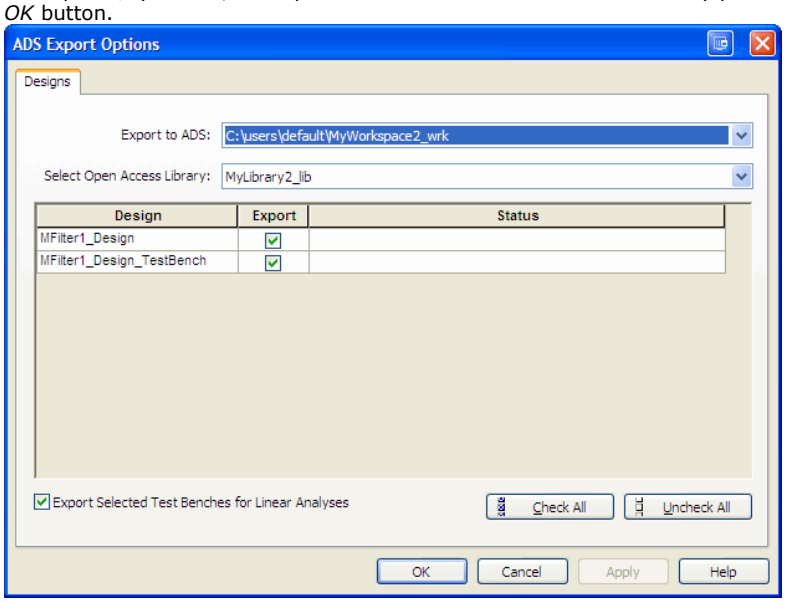
14. We will now export the schematic through ADS Link by selecting *File* > *Export* > *Export Schematic to ADS* .



15. Genesys insists that we save our workspace once.



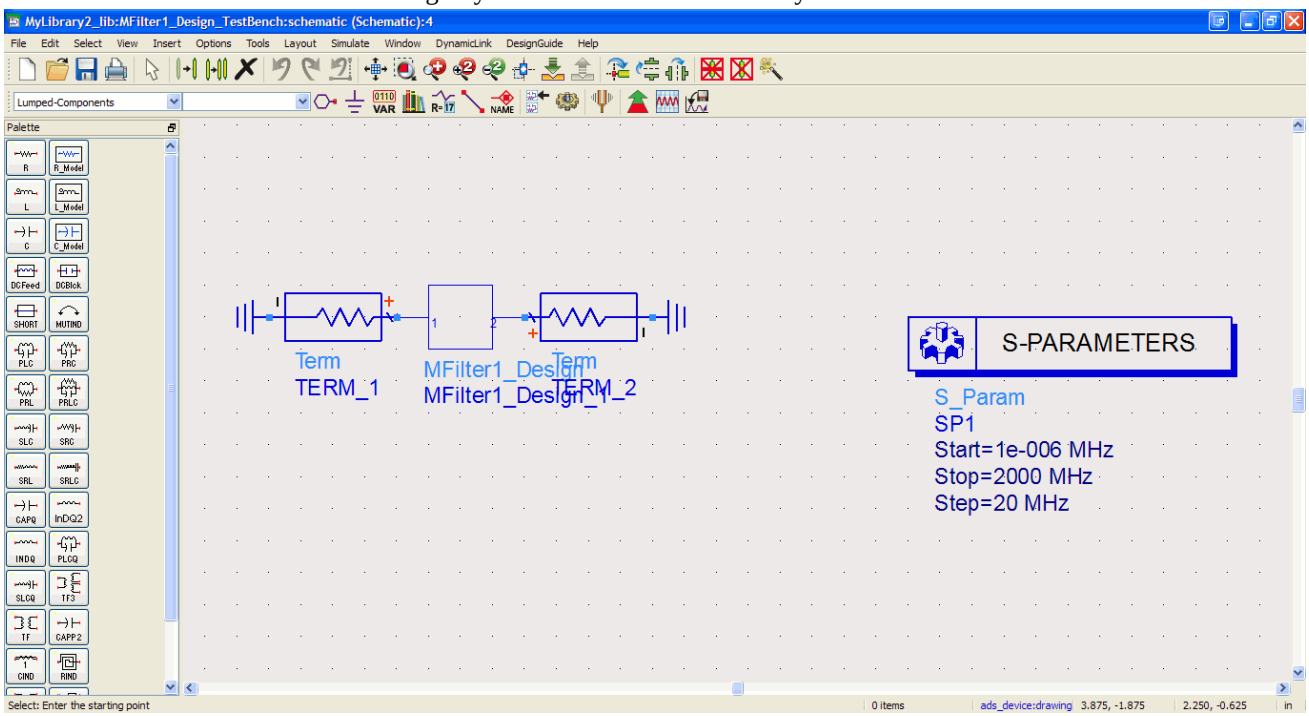
16. After saving our workspace (.wsx) into the prompted ADS workspace folder under workspaces/synthesis, we export our schematic with the test bench by pressing the *OK* button.



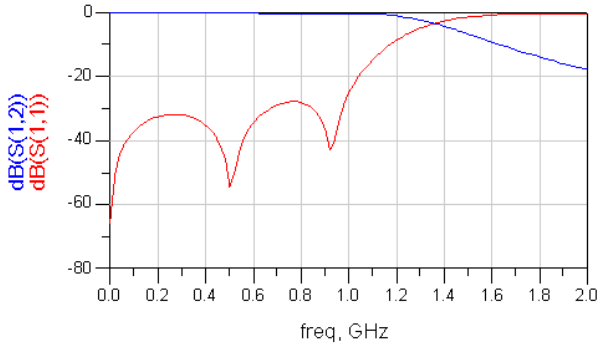
17. Our schematic and test bench designs are now available in ADS. GENESYS gives a message saying that the transfer is complete. For information on the location of files exported from GENESYS refer to Folders used by the GENESYS Synthesis/SPECTRASYS link.

> **Note**
> Open ADS windows will be closed during export from GENESYS, only the main ADS window will remain. Any changes in the ADS windows will be saved in memory, unsaved modifications will not be lost.

18. The test bench shows as follows:

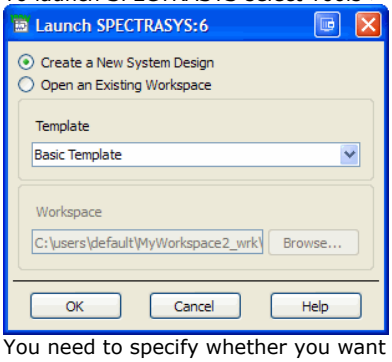


19. The schematic is a sub circuit between the two terminals in the test bench and can be viewed as a design.
20. Finally, after simulating the test bench, we plot the S11 and S12 characteristics of the synthesized microstrip filter.



Using SPECTRASYS from ADS

To launch SPECTRASYS select Tools > SPECTRASYS from the schematic window.



You need to specify whether you want to create a new design or open an existing Workspace. If creating a new System design, ADS asks what type of Template you'd like to use and then launches GENESYS to run SPECTRASYS. When you are finished, refer to Transferring schematics from GENESYS to ADS.

Note
Launching SPECTRASYS is a convenient way to start GENESYS with a blank schematic, even if you will not be using SPECTRASYS.

Note
See GENESYS documentation for examples and information on how to use SPECTRASYS.

Transferring schematics from GENESYS to ADS

You can transfer schematics from GENESYS to ADS using the *File* > *Export* > *Export Schematic to ADS* command in GENESYS. GENESYS displays a dialog box showing all instances of ADS with open workspaces. You first select the instance that you want (if you have more than one running), then you select which designs to export to ADS. When you click OK, the selected schematics are transferred to ADS. GENESYS posts a message saying that the transfer is successful. For information on locating the transferred files refer to Folders used by the GENESYS Synthesis/SPECTRASYS link.

Note
Open ADS windows will be closed during export from GENESYS, only the main ADS window will remain. Any changes in the ADS windows will be saved in memory, unsaved modifications will not be lost.

If no run-time link exists

GENESYS automatically establishes it, if possible. The link can be automatically established if there is an ADS session running and that session has a workspace open.

If ADS is not running

You should launch ADS. Once ADS is running and has an open workspace, go to GENESYS and select *File* > *Export* > *Export Schematic to ADS* .

If there is more than one ADS session running

GENESYS will ask you which session to link to. The ADS sessions are distinguished using the workspace name.